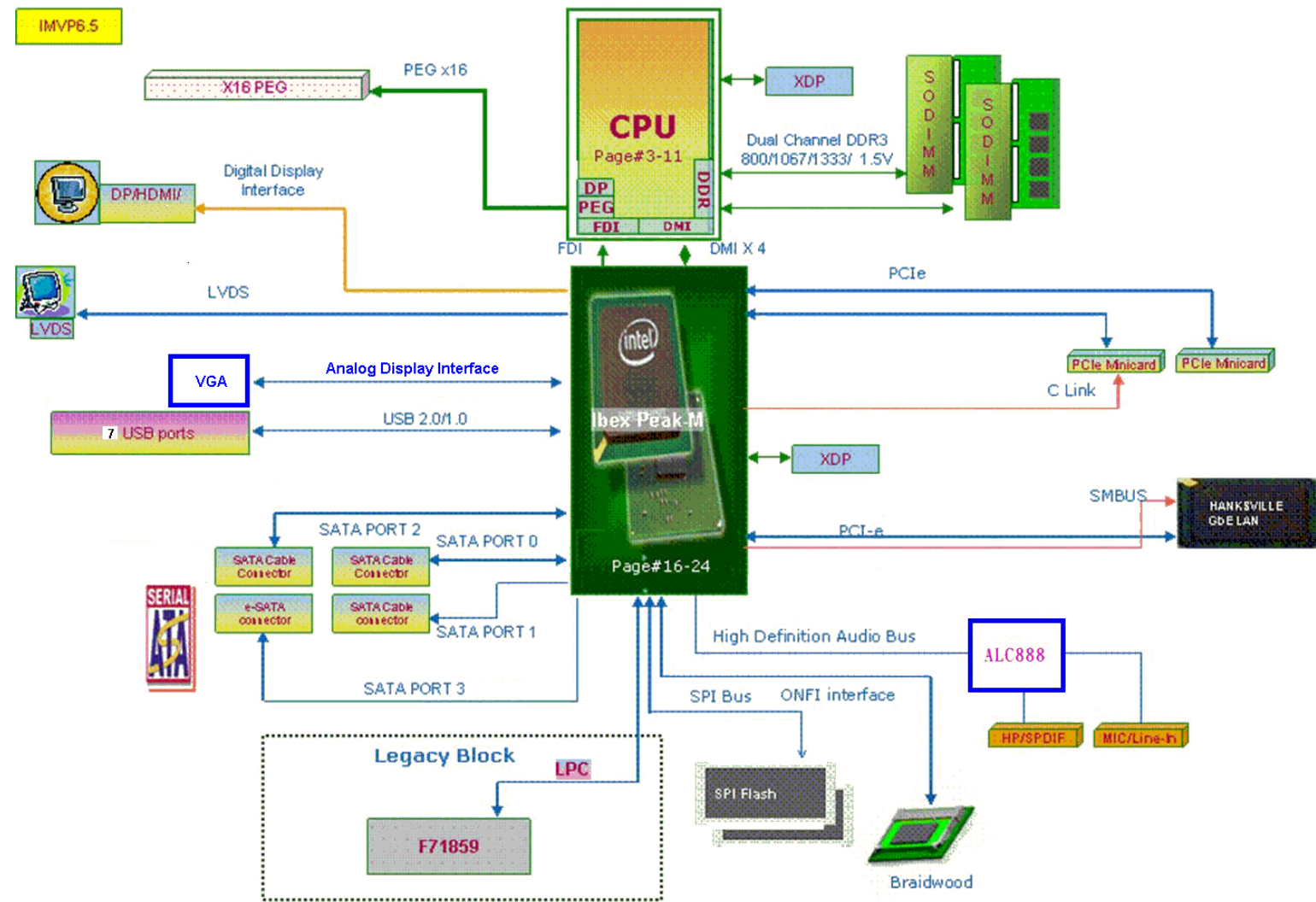


Page	Description
1	TITLE PAGE
2	NOTES
3	MCP (1 of 7)
4	MCP (2 of 7)
5	MCP (3 of 7)
6	MCP (4 of 7)
7	MCP (5 of 7)
8	MCP (6 of 7)
9	MCP (7 of 7)
10	FAN HEADERS
11	XDP (MCP)
12	PROCESSOR STRAPS
13	DDR3 SODIMM
14	DDR3 SODIMM
15	IBEXPEAK (1 of 9)
16	IBEXPEAK (2 of 9)
17	IBEXPEAK (3 of 9)
18	IBEXPEAK (4 of 9)
19	IBEXPEAK (5 of 9)
20	IBEXPEAK (6 of 9)
21	IBEXPEAK (7 of 9)
22	IBEXPEAK (8 of 9)
23	IBEXPEAK (9 of 9)
24	DISPLAYPORT-HDMI
25	LVDS
26	BRAIDWOOD
27	USB 2.0 (1 of 2)
28	USB 2.0 (2 of 2)
29	MINICARD
30	SATA
31	LAN HANKSVILLE
32	SPI
33	CKSOS
34	IBEXPEAK-M XDP
35	F71859 SIO
36	PCI-E x16
37	TPS6125 SYSTEM POWER VR
38	+12V ADDR3 VR
39	V1.1 VR
40	GRAPHICS CORE VR
41	IMVP-6.5
42	DISCHARGE CIRCUITS
43	STANBY UP SEQUENCE
44	SLEEP CONTROL
45	POWER SEQUENCE LOGIC
46	POWER UP SEQUENCE
47	PCH STRAPS
48	VGA
49	REVISION HISTORY
50	REVISION HISTORY1
51	REVISION HISTORY2
52	



CALPELLA ON DESKTOP ENABLING BOARD

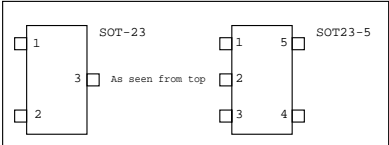
SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails			
POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
+V12A	12V	S0/M0, (S3-S5)/M1, (S3-S5)/M-off	
+V12S	12V	S0/M0	
+V5A	5V	S0/M0, (S3-S5)/M1, (S3-S5)/M-off	
+V5	5V	S0/M0, S3/M1, S3/M-off	
+V5S	5V	S0/M0	
+V3_3A	3.3V	S0/M0, (S3-S5)/M1, (S3-S5)/M-off	
+V3_3M	3.3V	S0/M0, (S3-S5)/M1, S3/(M-off w/WOL_EN)	LAN
+V3_3M_CK505	3.3V	S0/M0, (S3-S5)/M1	Clock, MCH
+V3_3	3.3V	S0/M0, S3/M1, S3/M-off	
+V3_3S	3.3V	S0/M0	
+V1_5	1.8V	S0/M0, (S3-S5)/M1, S3/M-off	
+V1_5S	1.5V	S0/M0	DDR core
+V1_05M	1.05V	S0/M0, (S3-S5)/M1	
+V1_05S	1.05V	S0/M0	GMCH, ICH core, and FSB rail
+V0_75	0.9V	S0/M0, (S3-S5)/M1, S3/M-off	DDR command & control pull up.
+VCC_CORE	0.35V-1.5V	S0/M0	CPU core rail
+VCC_GFXCORE	0.7V-1.25V	S0/M0	GMCH Graphics core rail

Net Naming Conventions

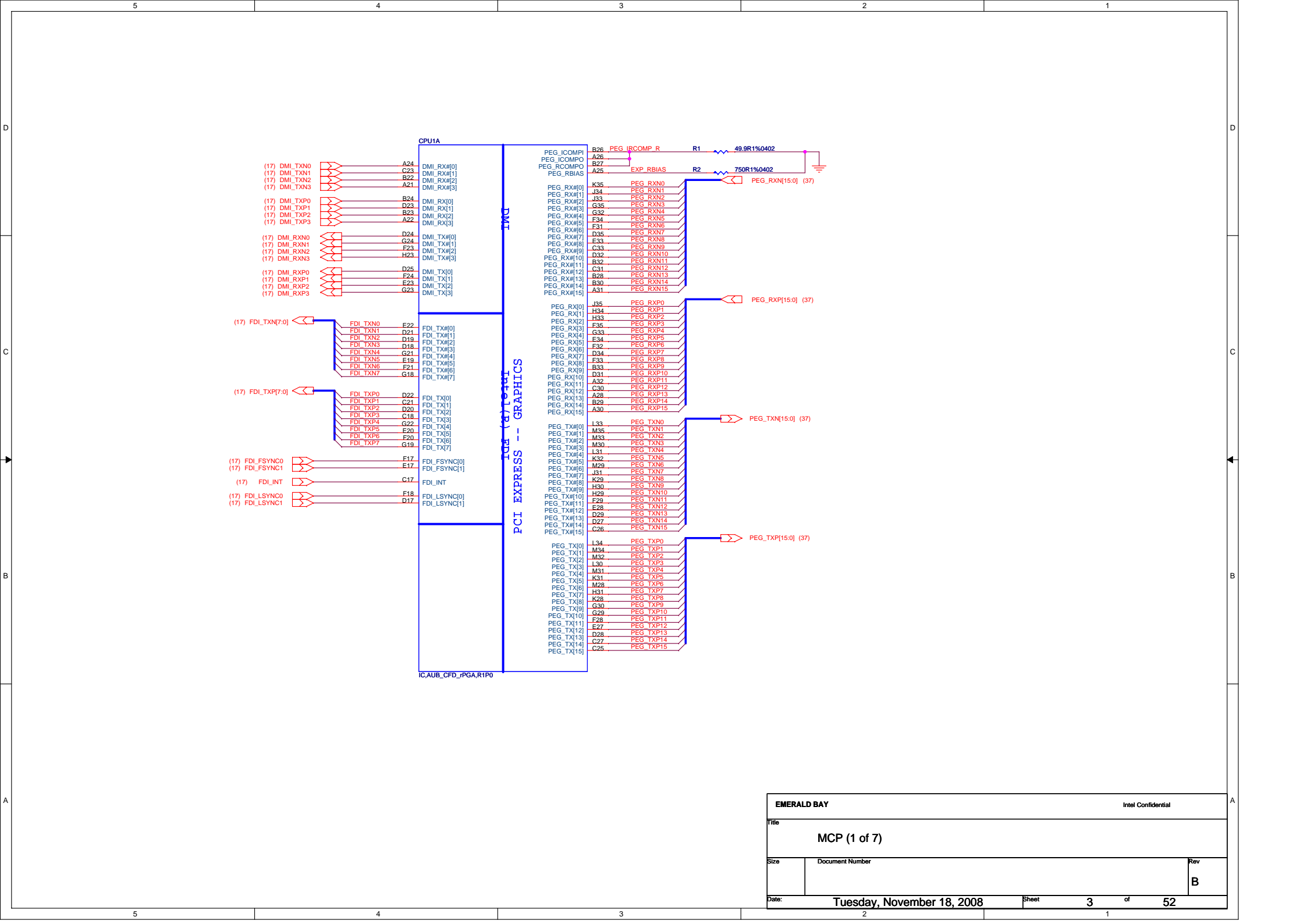
Suffix
= Active Low Signal
Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

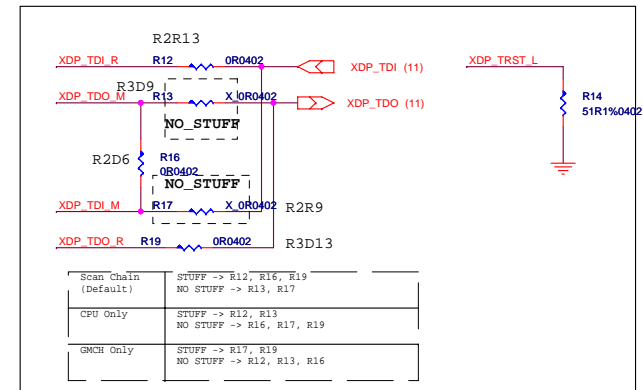
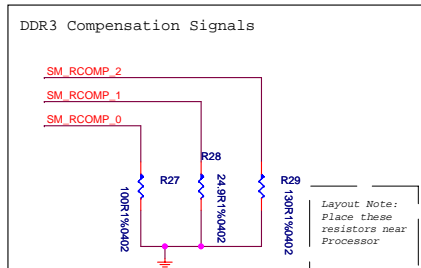
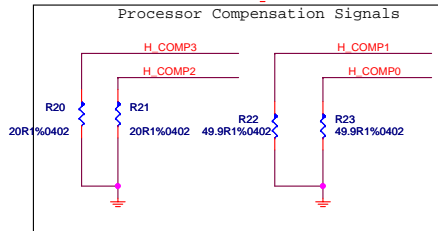
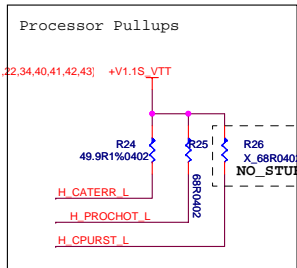
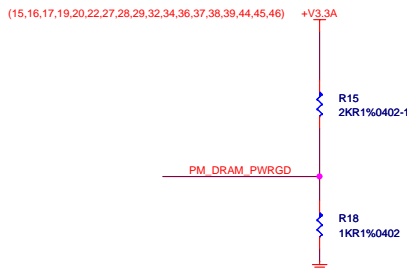
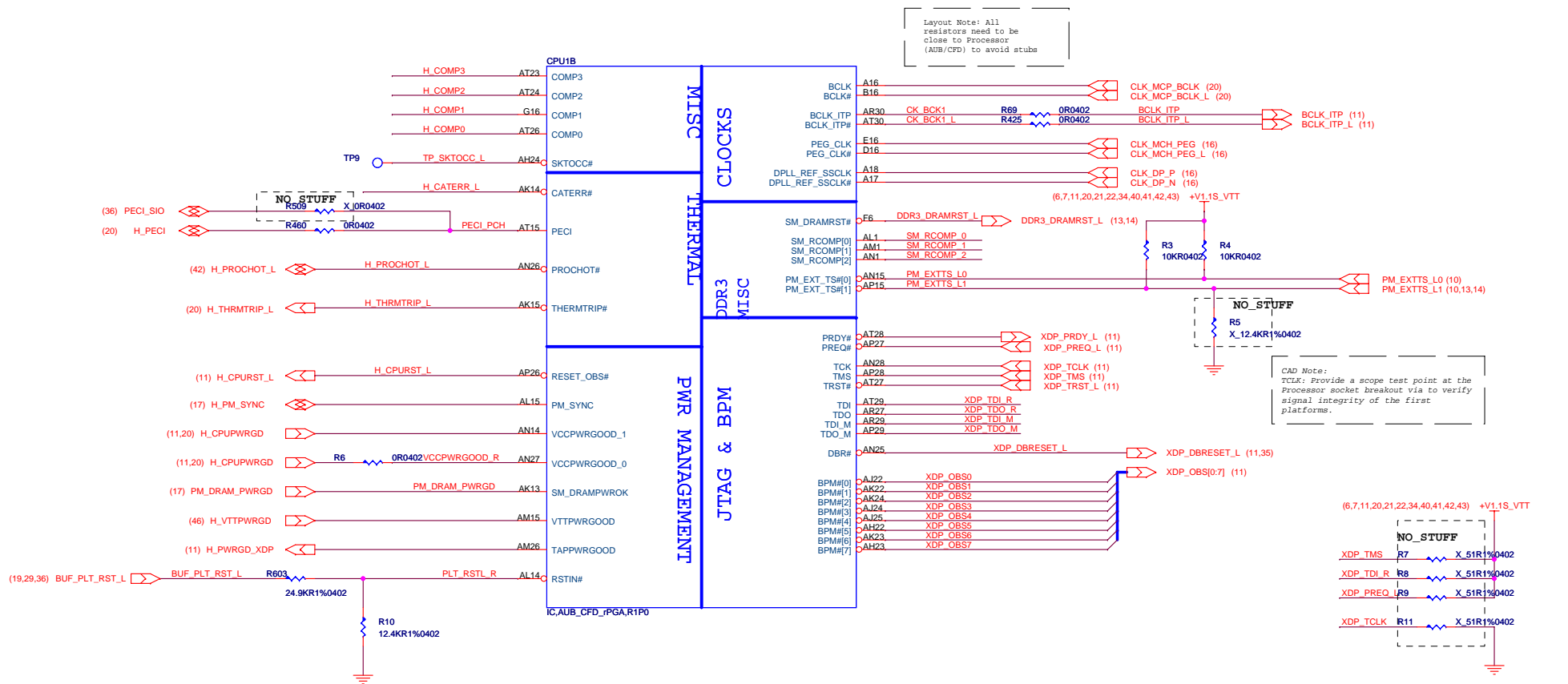
PCB Footprints



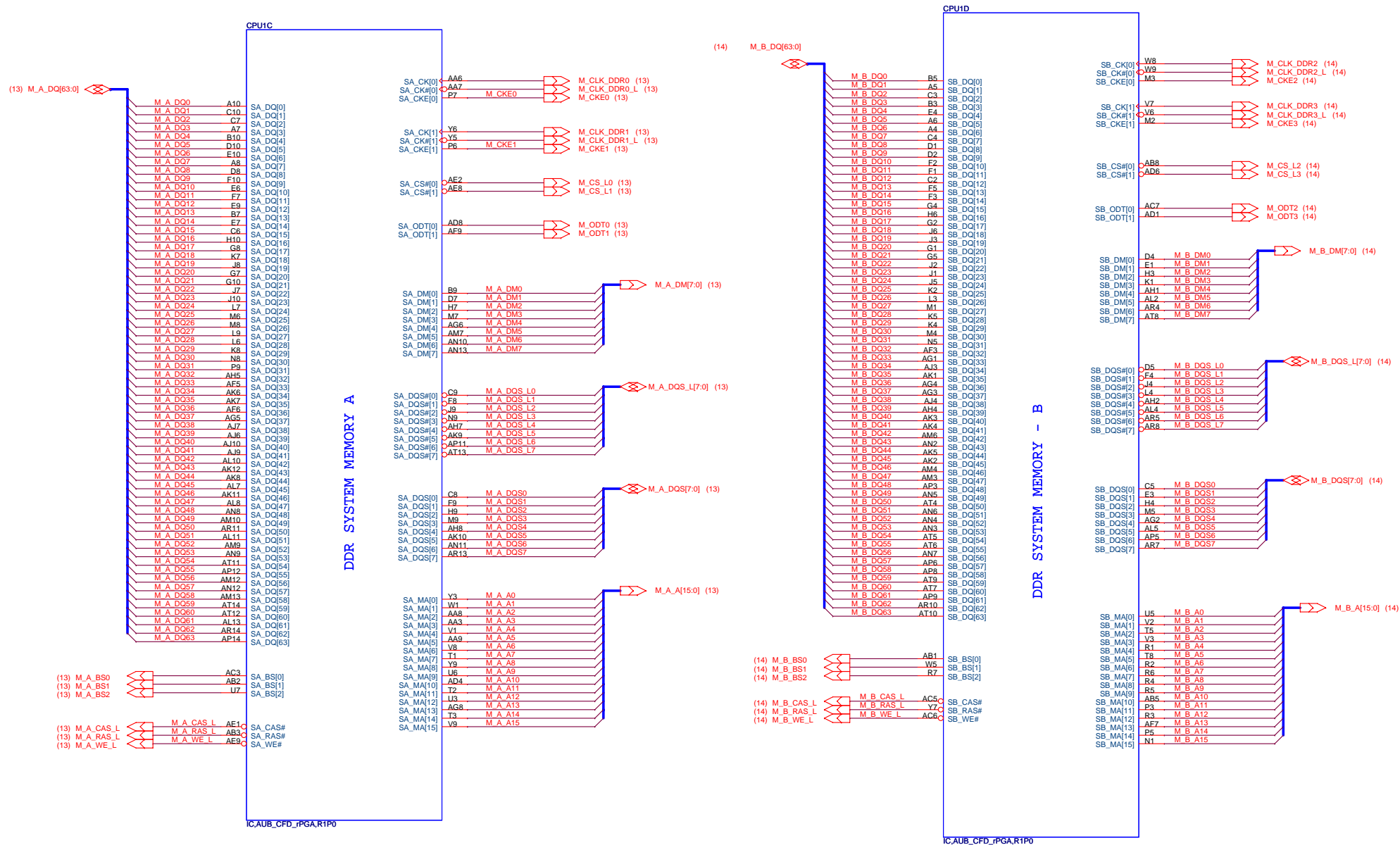
Power States	SLP_S3#	S4_STATE#	SLP_S4#	SLP_S5#	SLP_M#	+V*A	+V3.3M_WOL	+V1.05M	+V3.3M	+V1.5/+V0.75	+V5/+V3.3	+V*S	Clocks
S0 (Full on)/M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON	ON	ON	ON
S3 (Suspend to RAM)/M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON	ON	OFF	only MCH BCLK
S3 (Suspend to RAM)/Moff	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	OFF	OFF	ON	ON	OFF	OFF
S3 (Suspend to RAM)/Moff w/WOL_EN	LOW	HIGH	HIGH	HIGH	LOW	ON	ON	OFF	OFF	ON	ON	OFF	OFF
S4 (Suspend to Disk)/M1	LOW	LOW	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON	OFF	OFF	only MCH BCLK
S5 (Soft Off)/M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	ON	ON	ON	OFF	OFF	only MCH BCLK
S4 (Suspend to Disk)/Moff	LOW	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
S5 (Soft Off)/Moff	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF

EMERALD BAY		Intel Confidential
Title		
NOTES		
Size	Document Number	Rev
A		B
Date:	Tuesday, November 18, 2008	Sheet 2 of 52



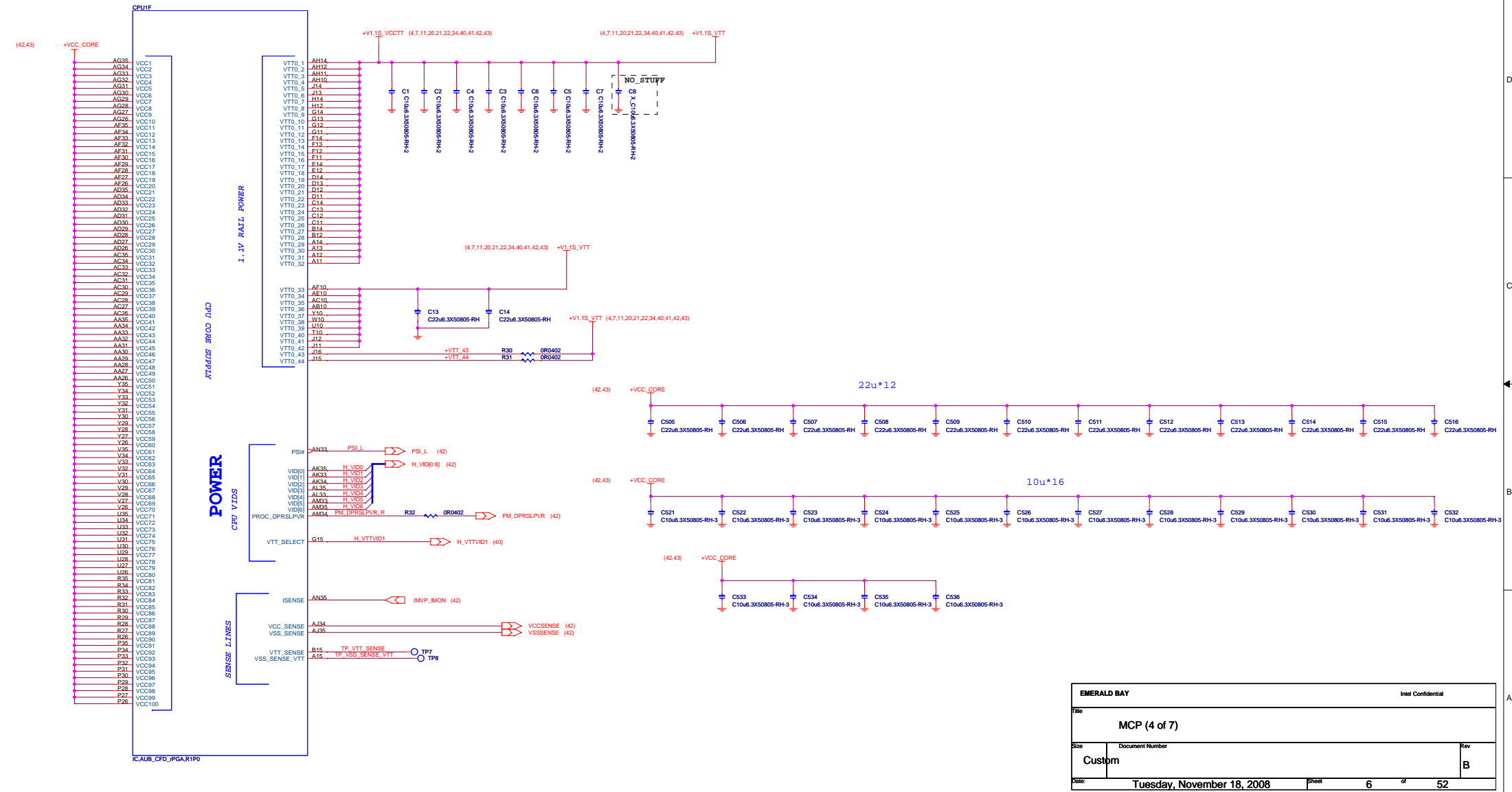


AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



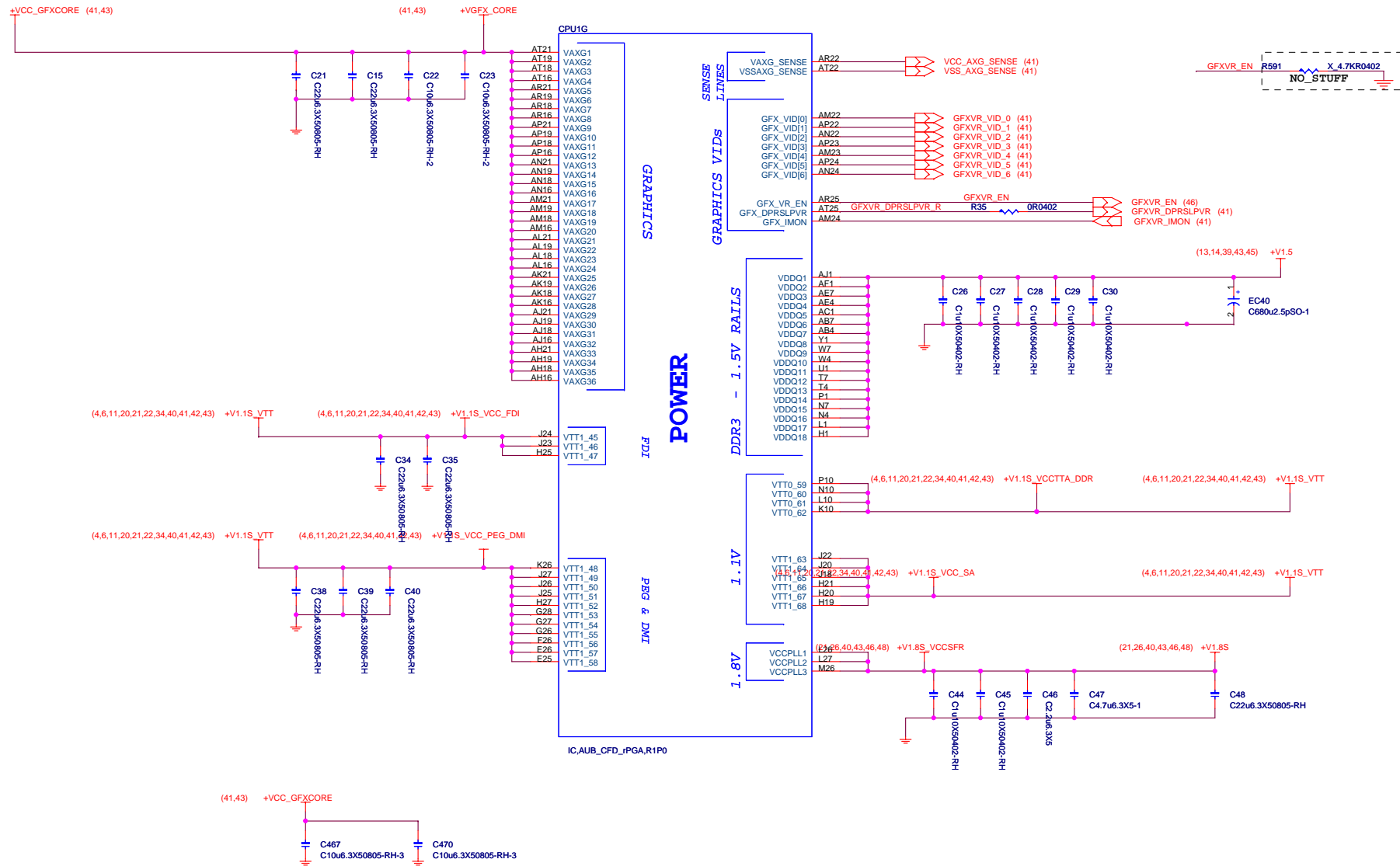
EMERALD BAY		Intel Confidential
Title		
MCP (3 of 7)		
Size	Document Number	Rev
A		B
Date:	Tuesday, November 18, 2008	Sheet 5 of 52

AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

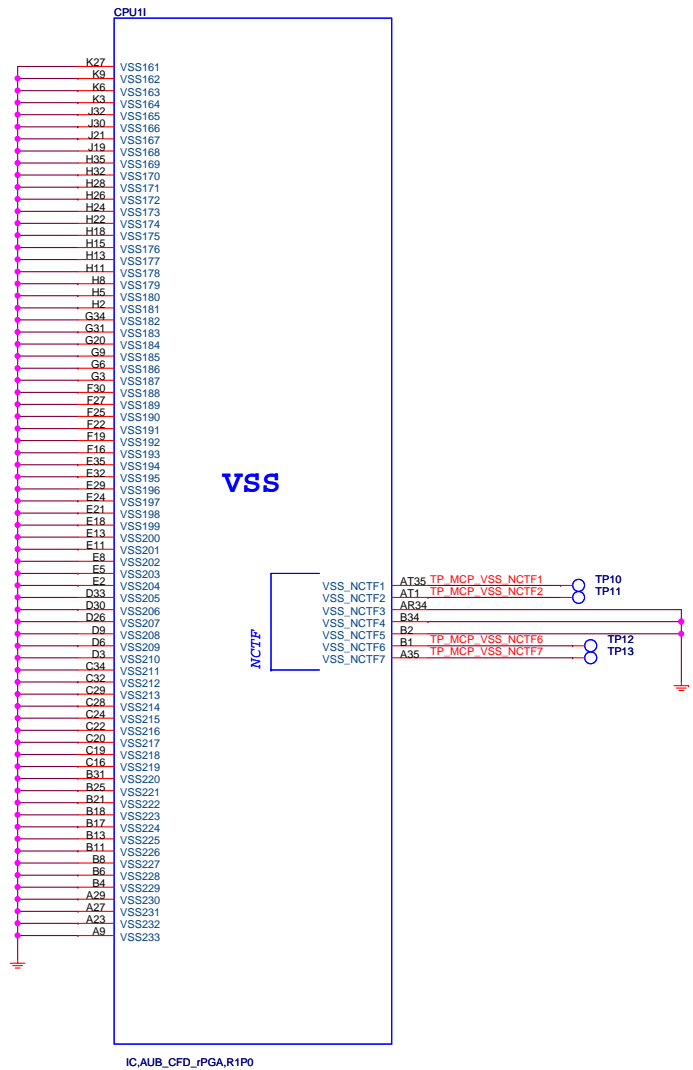
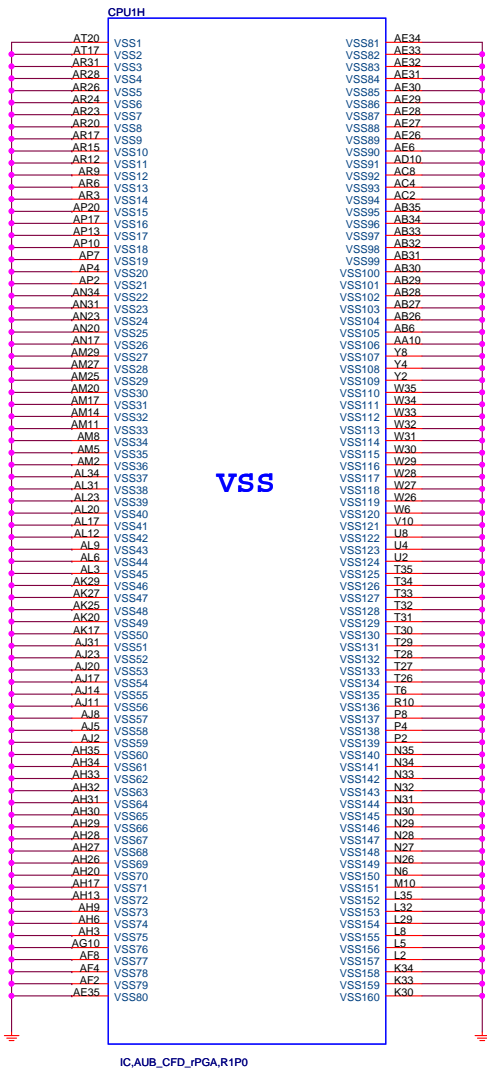


EMERALD BAY		Intel Confidential	
File		MCP (4 of 7)	
Size	Document Number	Rev	
Custom		B	
Date:	Tuesday, November 18, 2008		Sheet 6 of 52

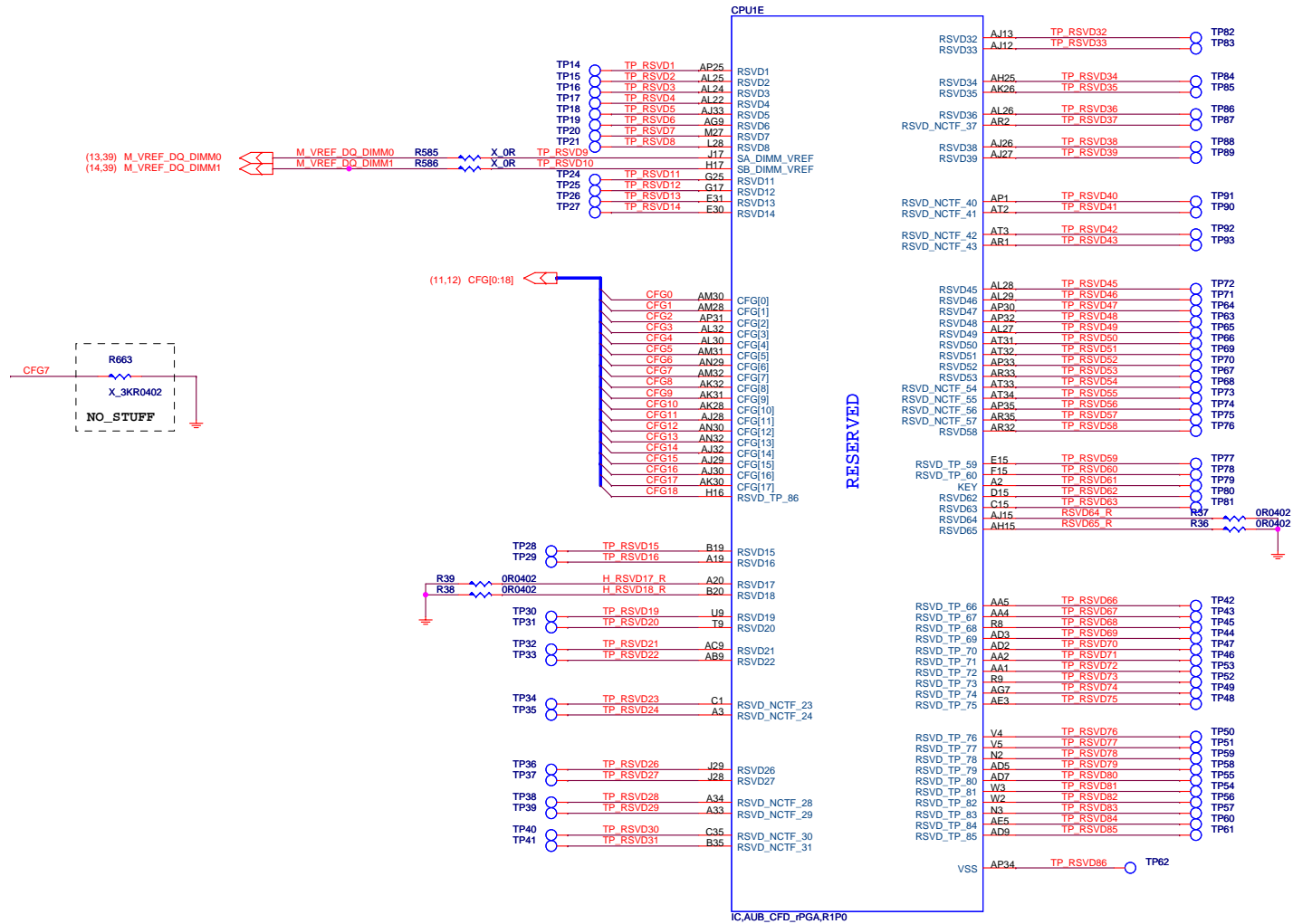
AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)



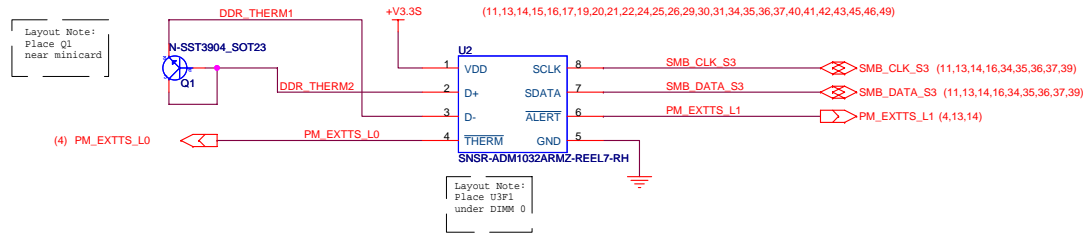
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



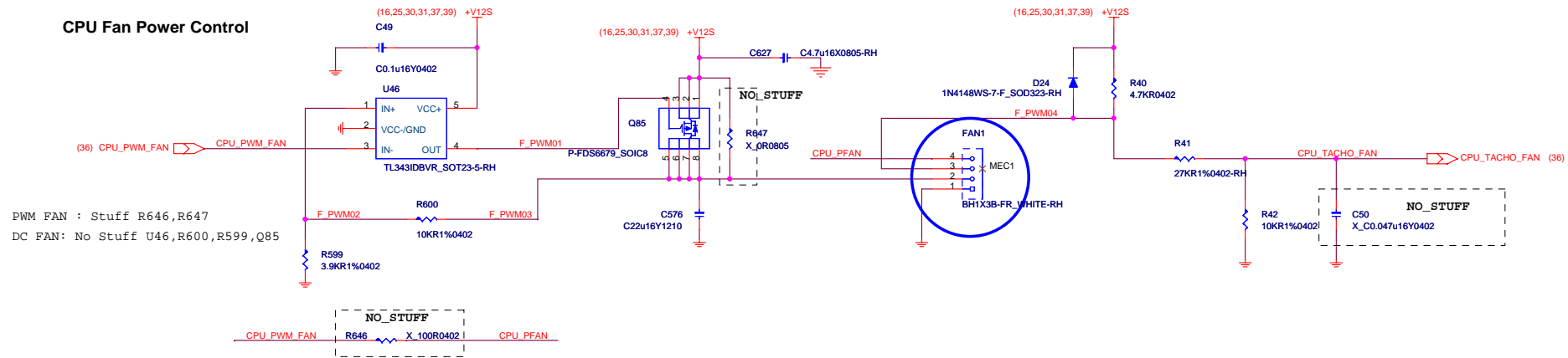
AUBURNDALE/CLARKSFIELD PROCESSOR (RESERVED)



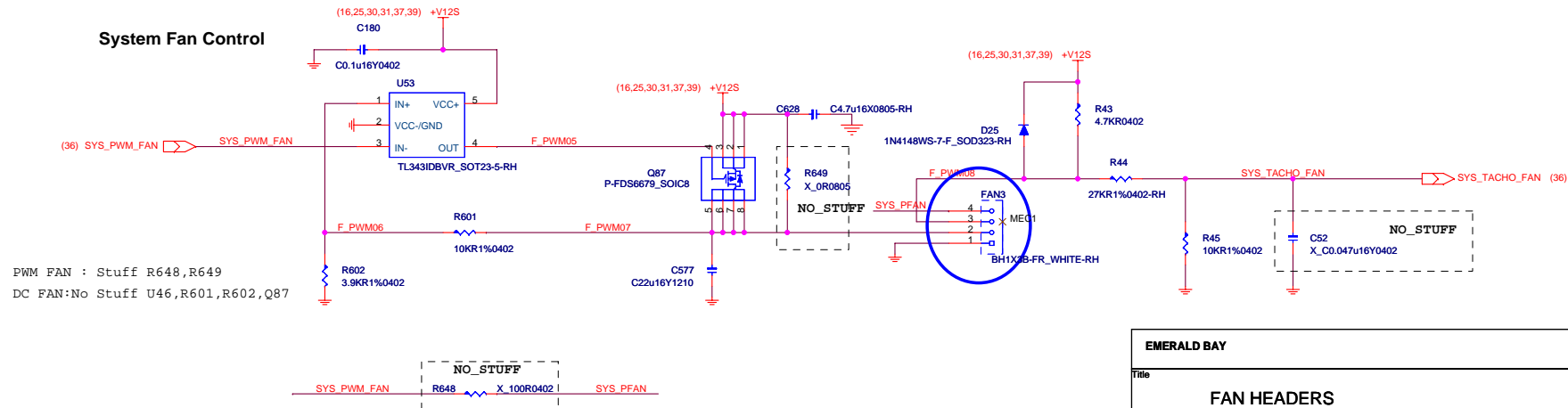
On Board DDR3 Thermal Sensor



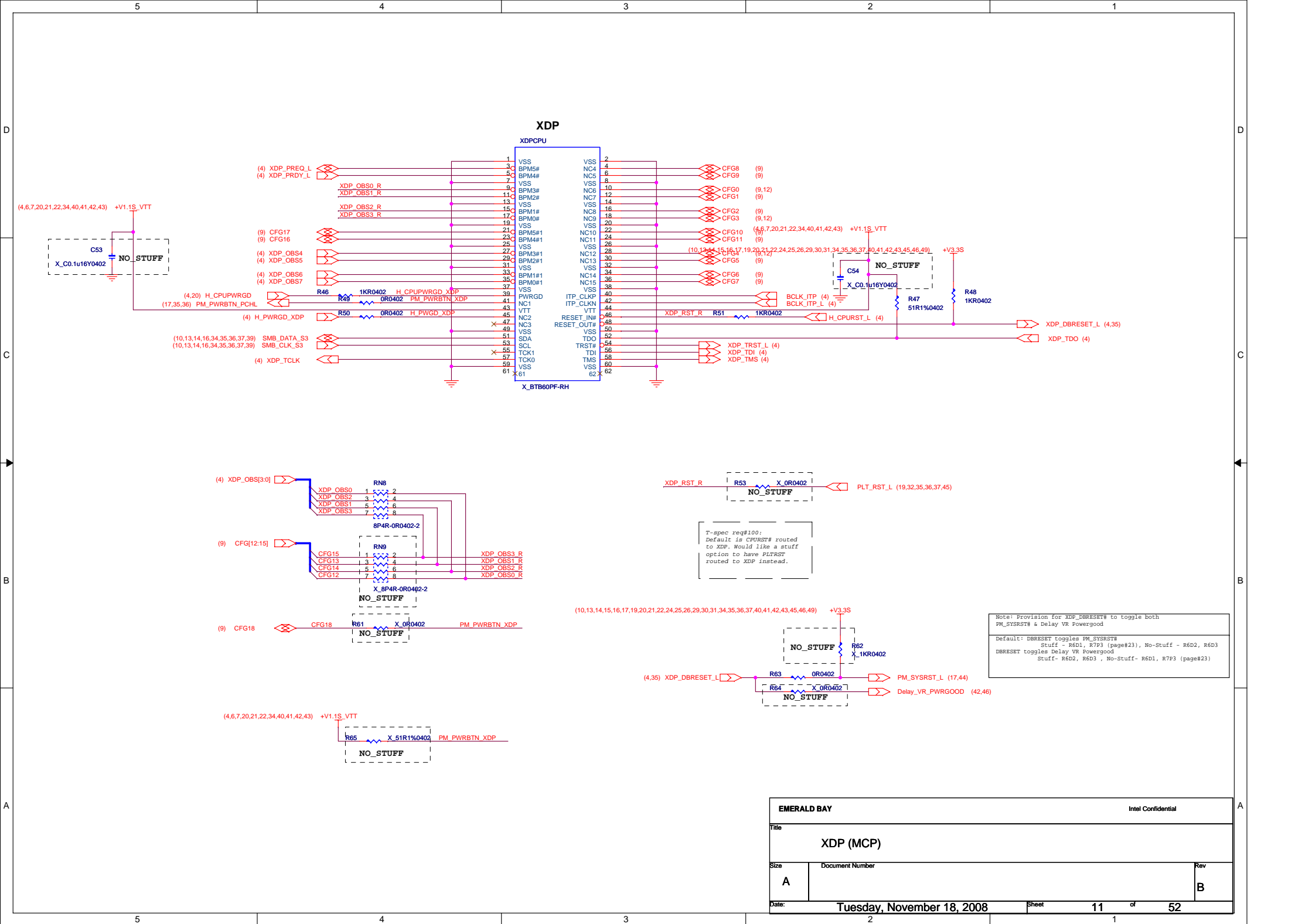
CPU Fan Power Control

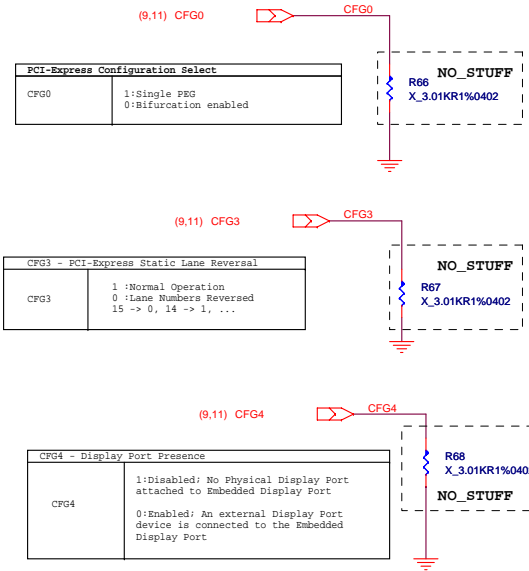


System Fan Control



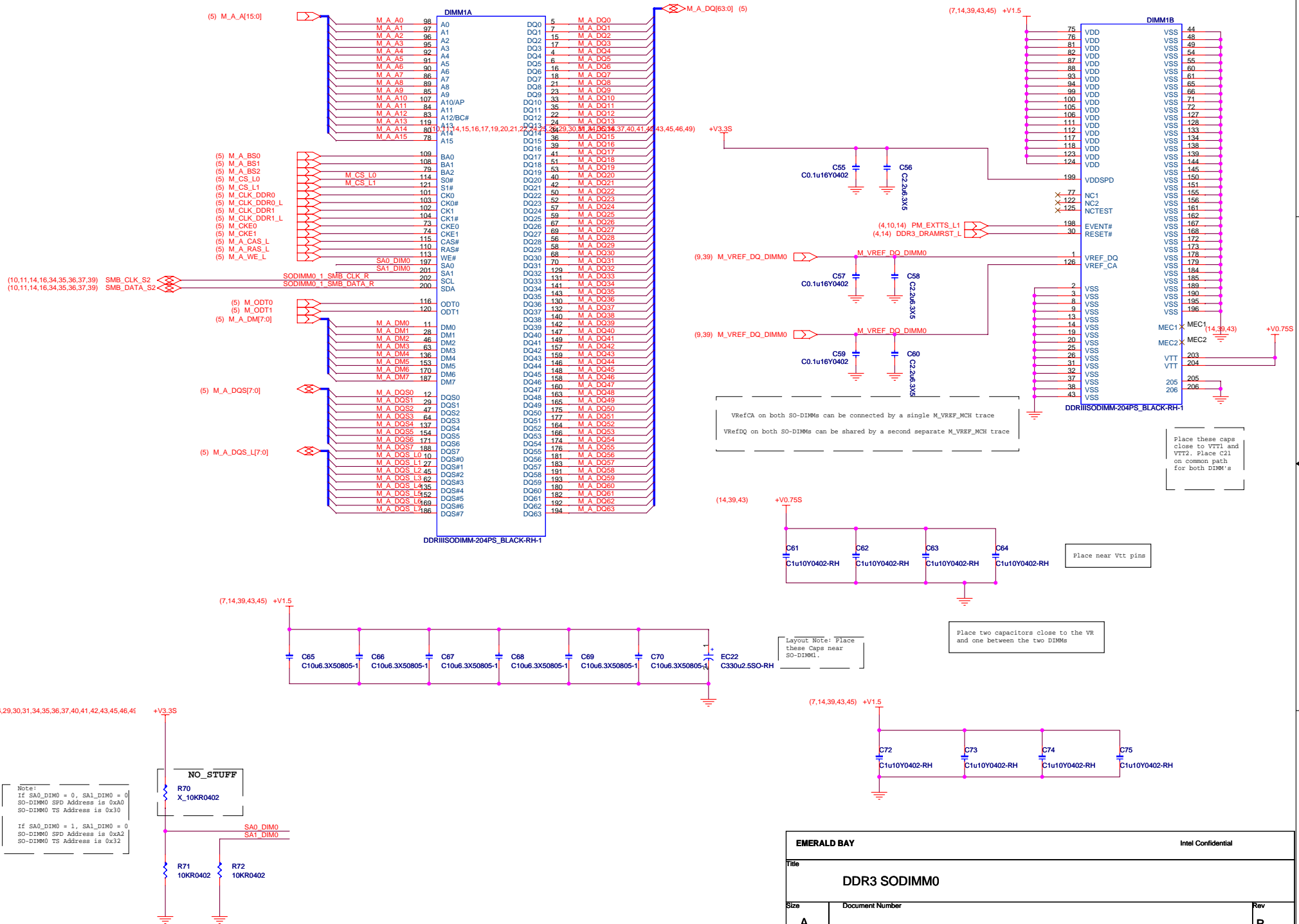
EMERALD BAY		Intel Confidential	
Title			
FAN HEADERS			
Size	Document Number		Rev
A			B
Date:	Tuesday, November 18, 2008	Sheet	10 of 52



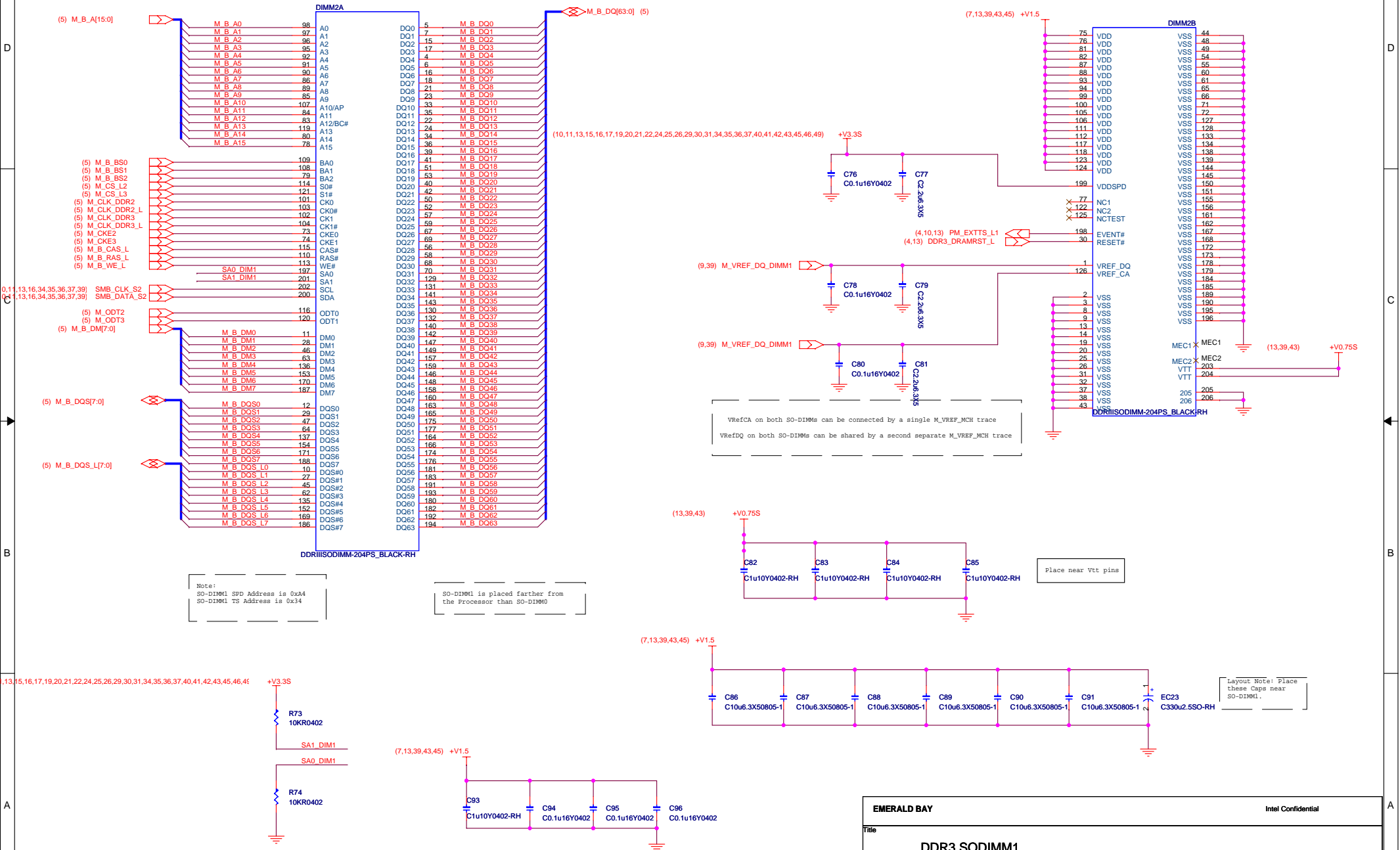


Layout Note:
Location of all CFG strap resistors needs
to be close to trace to minimize stub

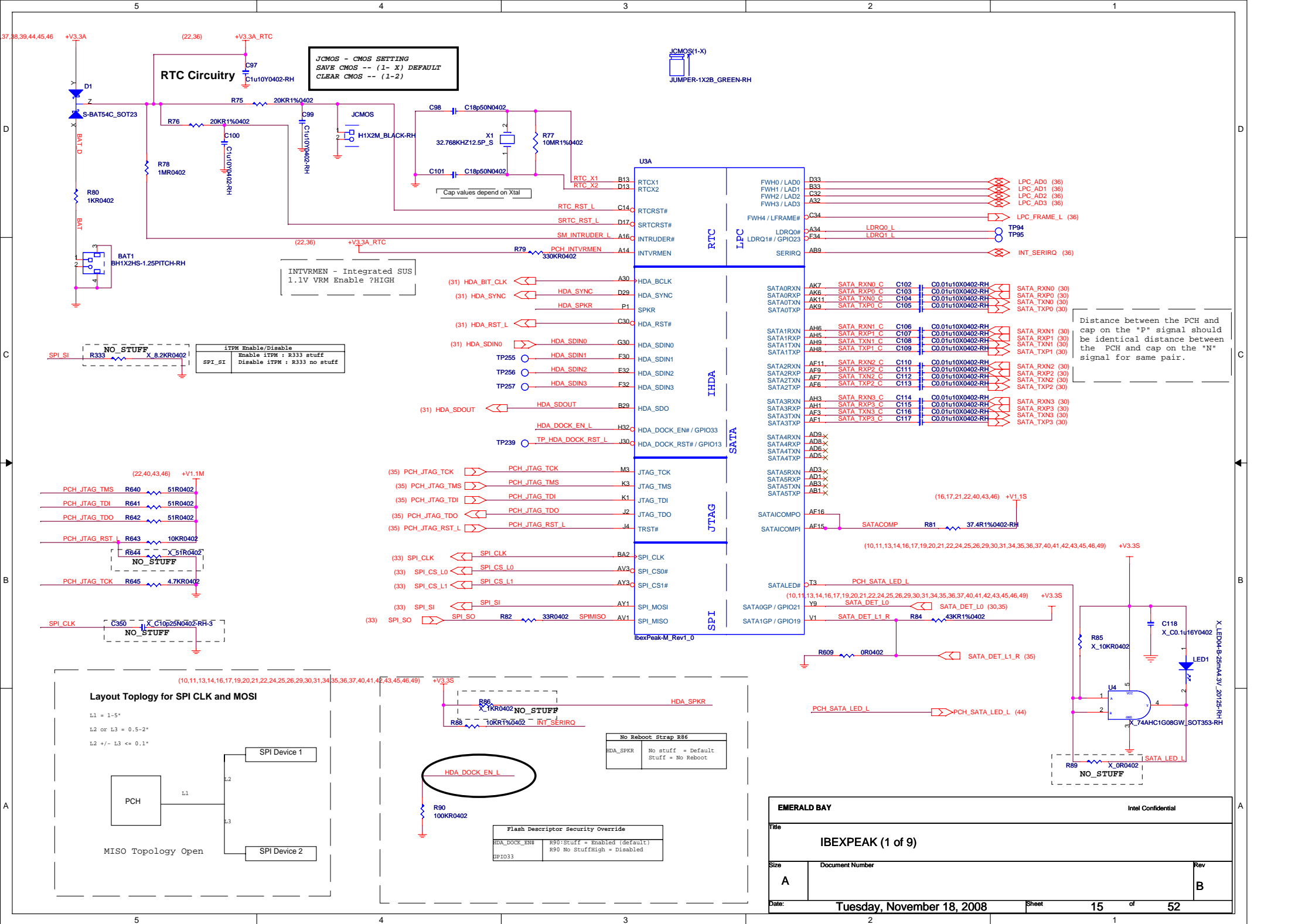
Channel A High :9.2mm

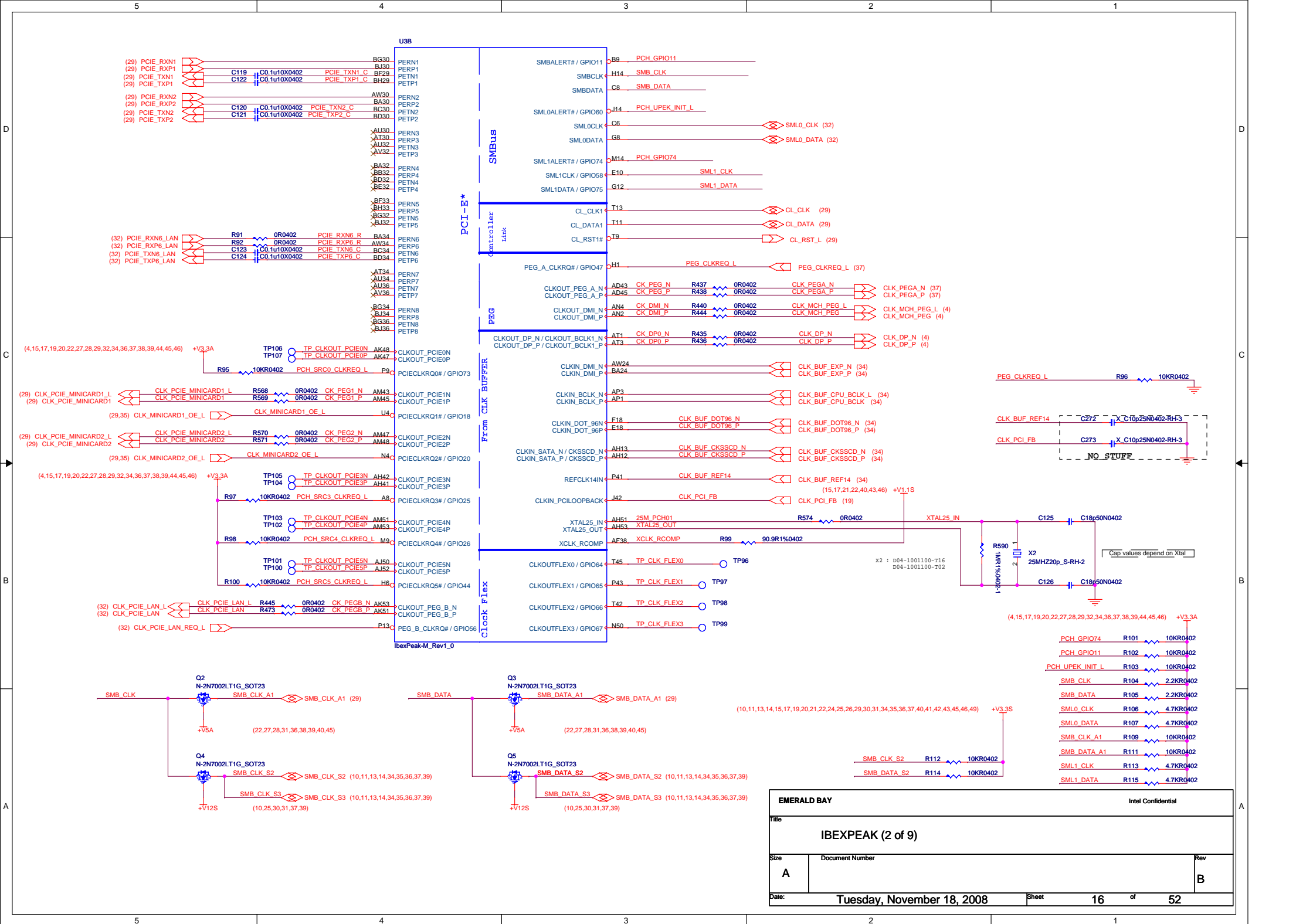


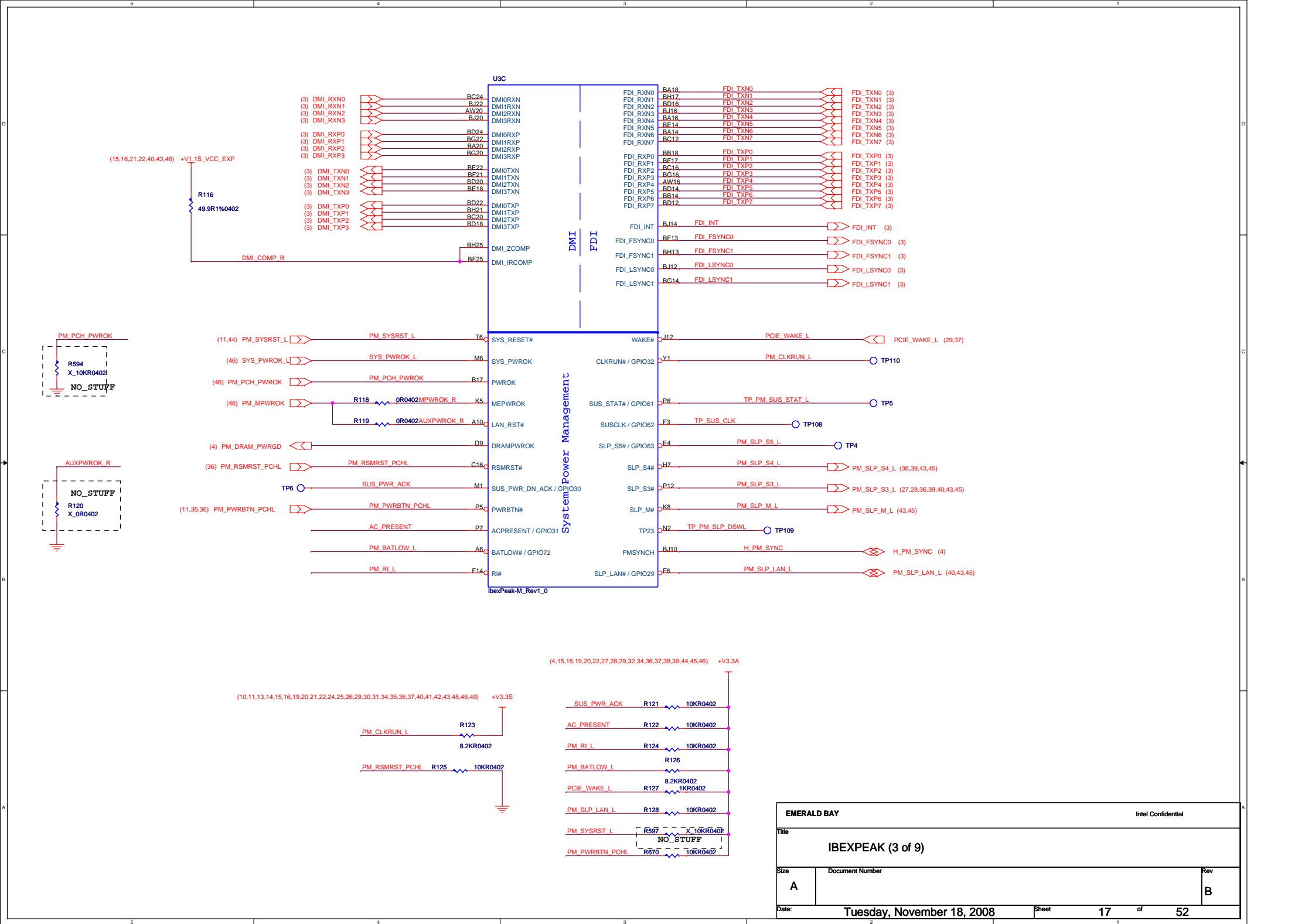
Channel B High :5.2mm

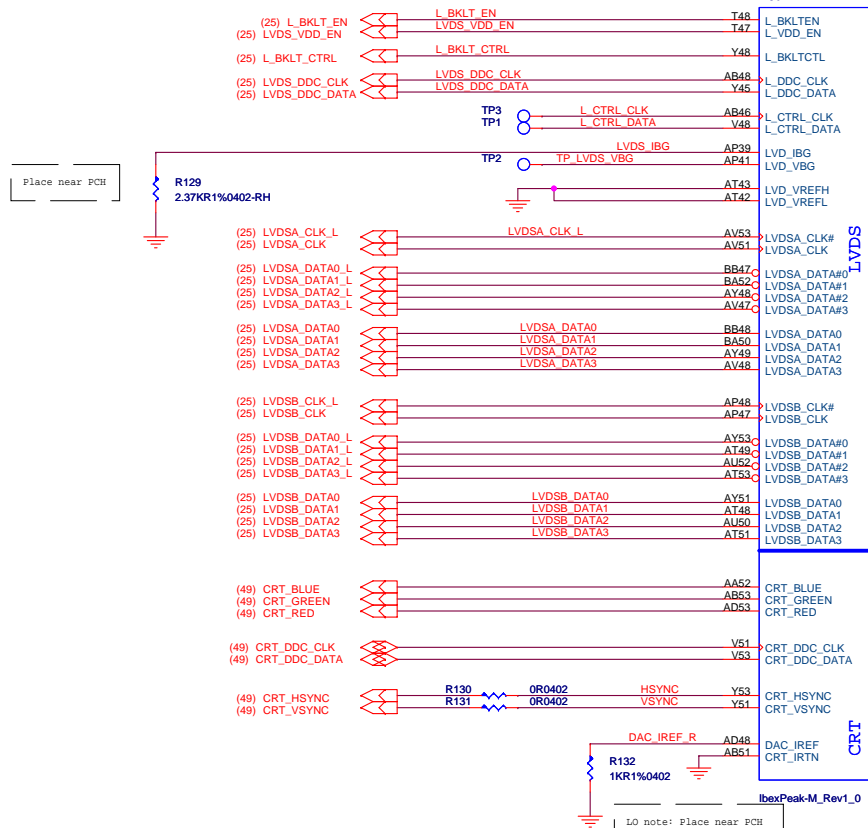


EMERALD BAY			Intel Confidential
Title			
DDR3 SODIMM1			
Size	Document Number		Rev
A			B
Date:	Tuesday, November 18, 2008		Sheet 14 of 52

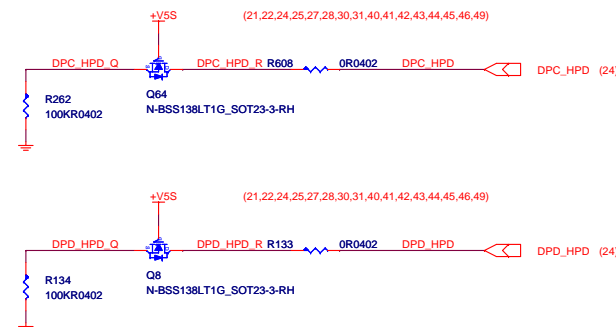
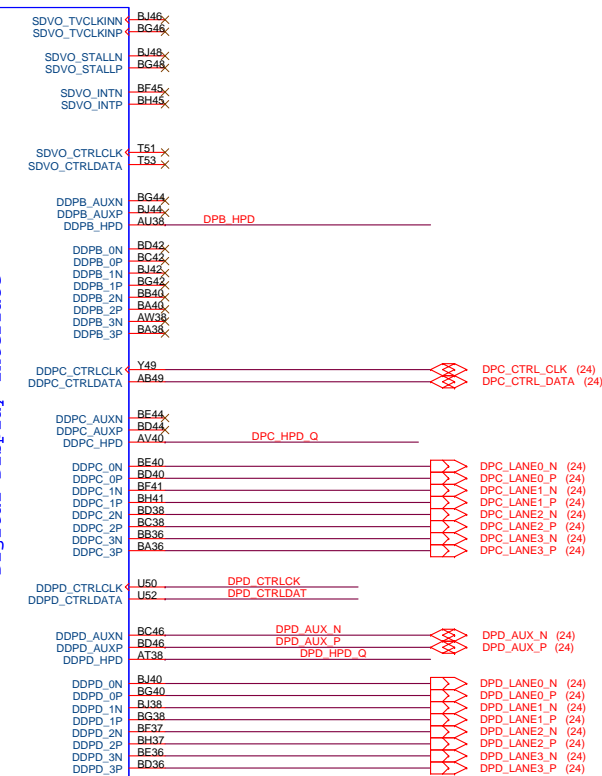


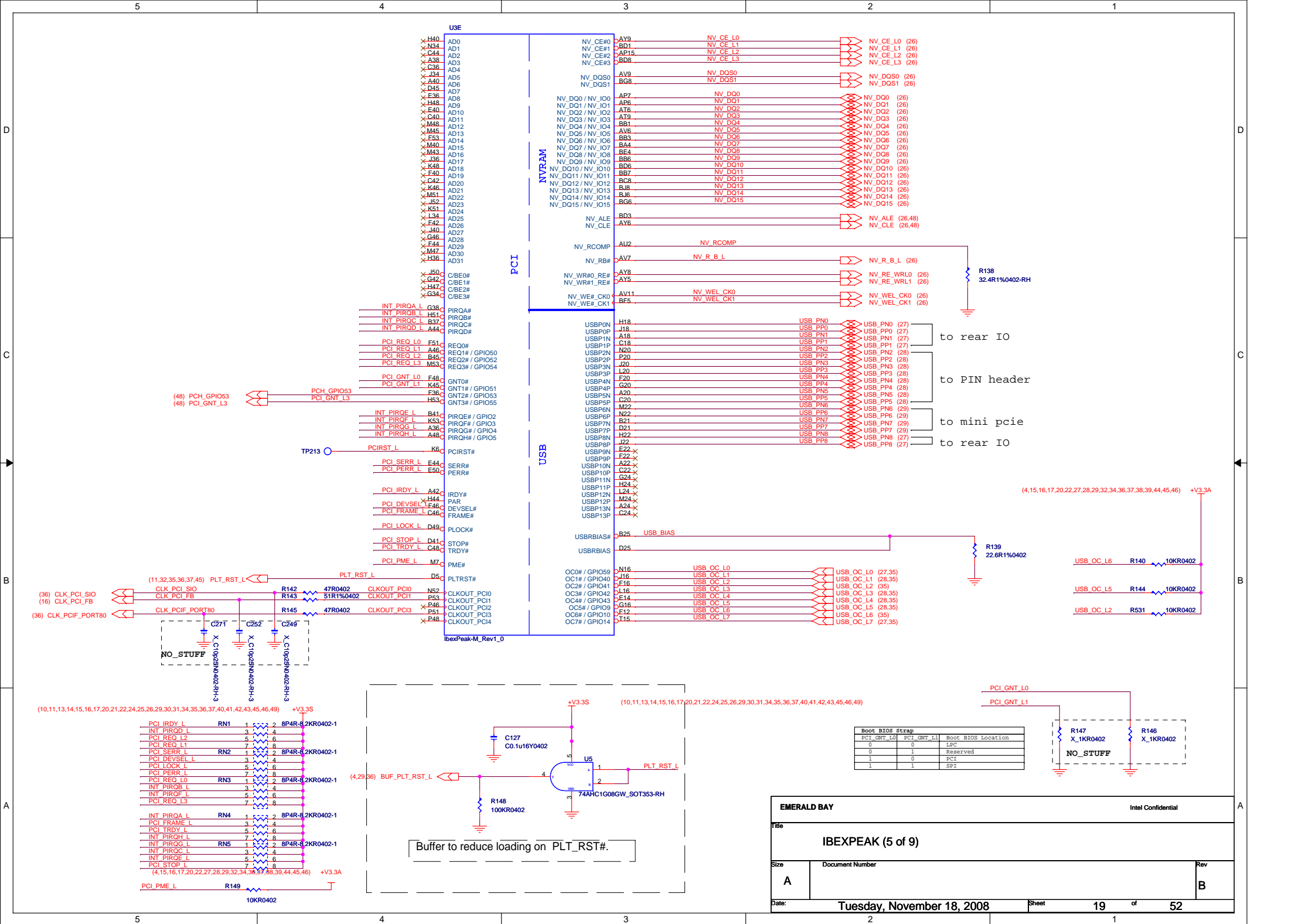


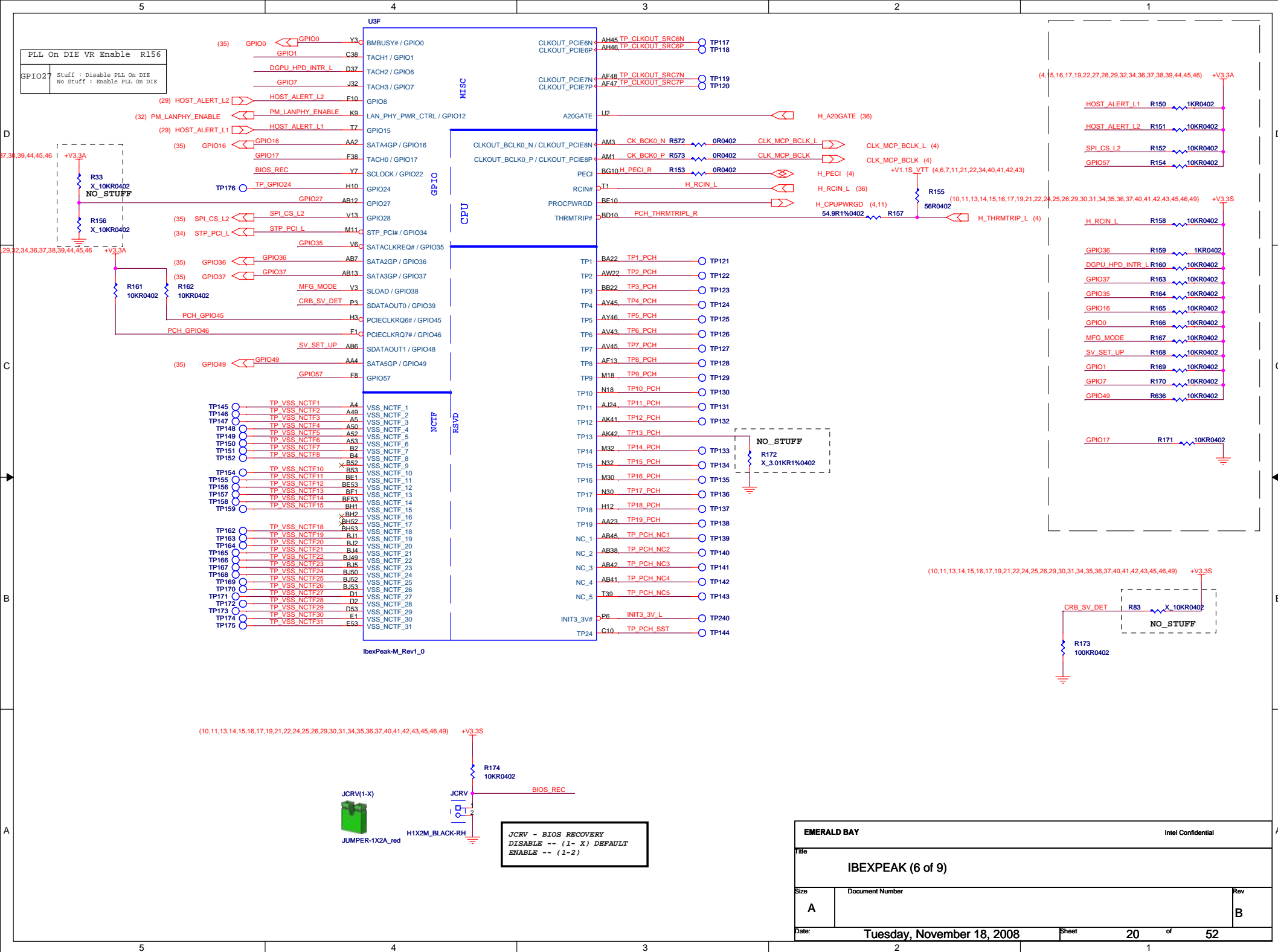


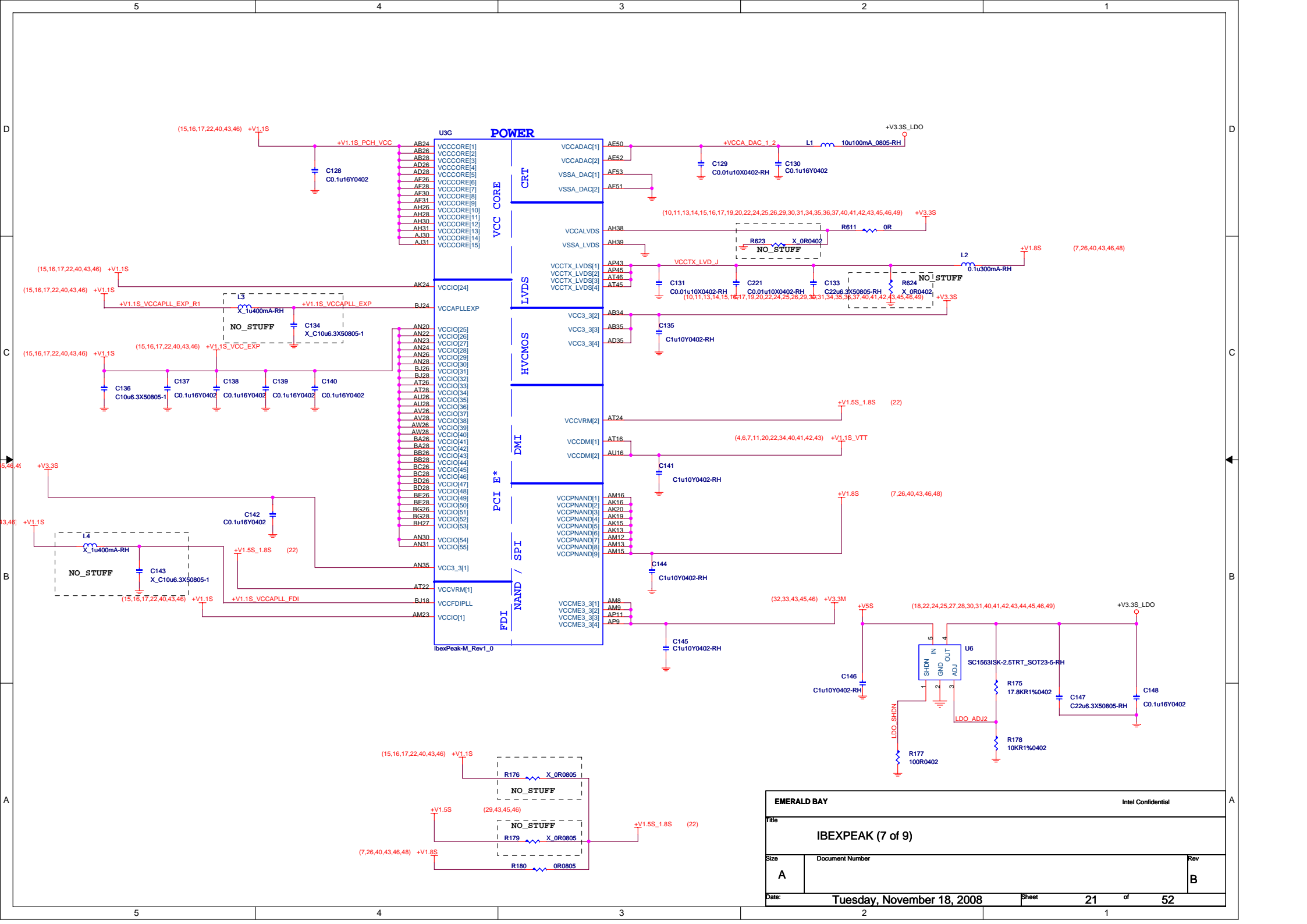


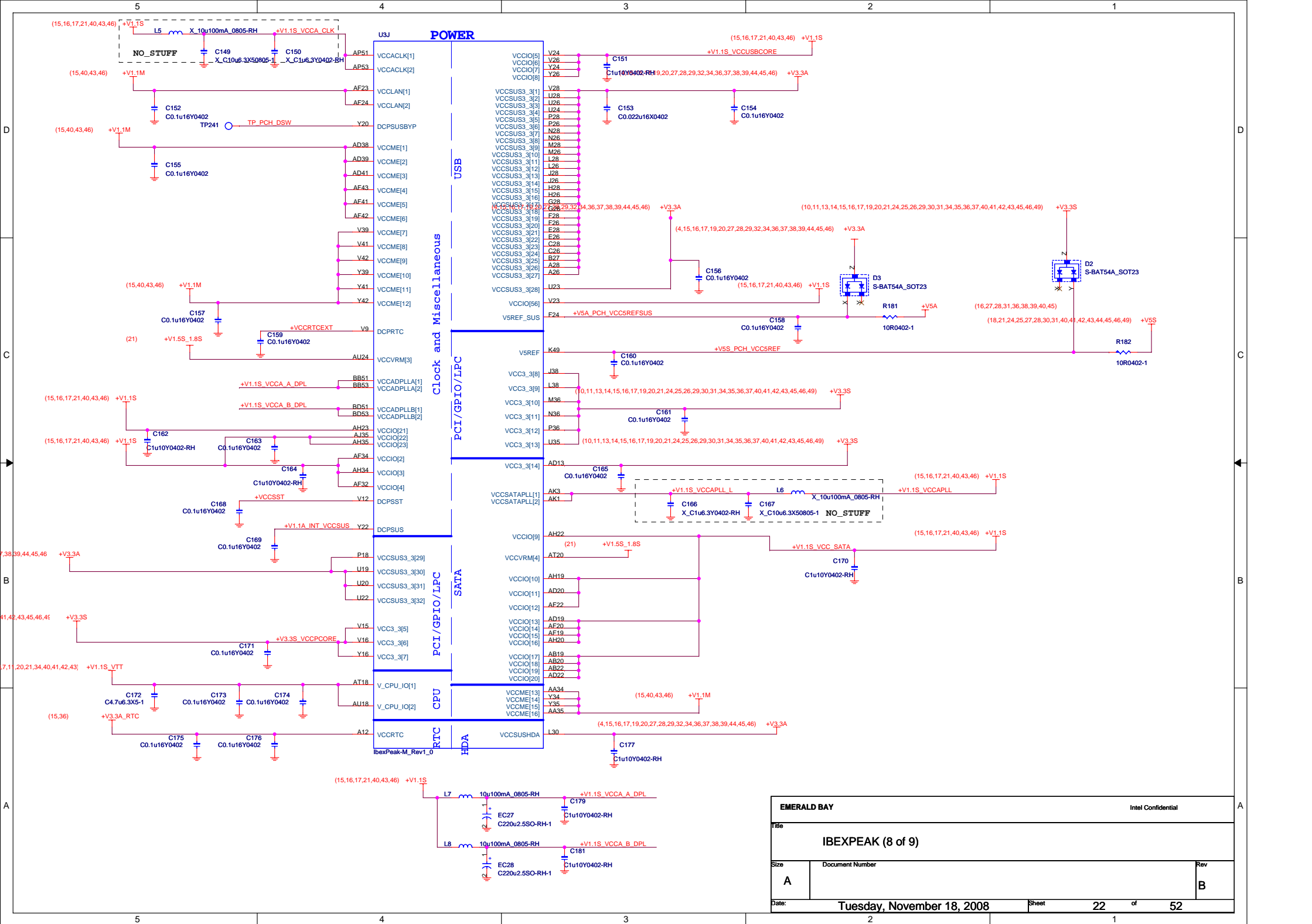
Digital Display Interface

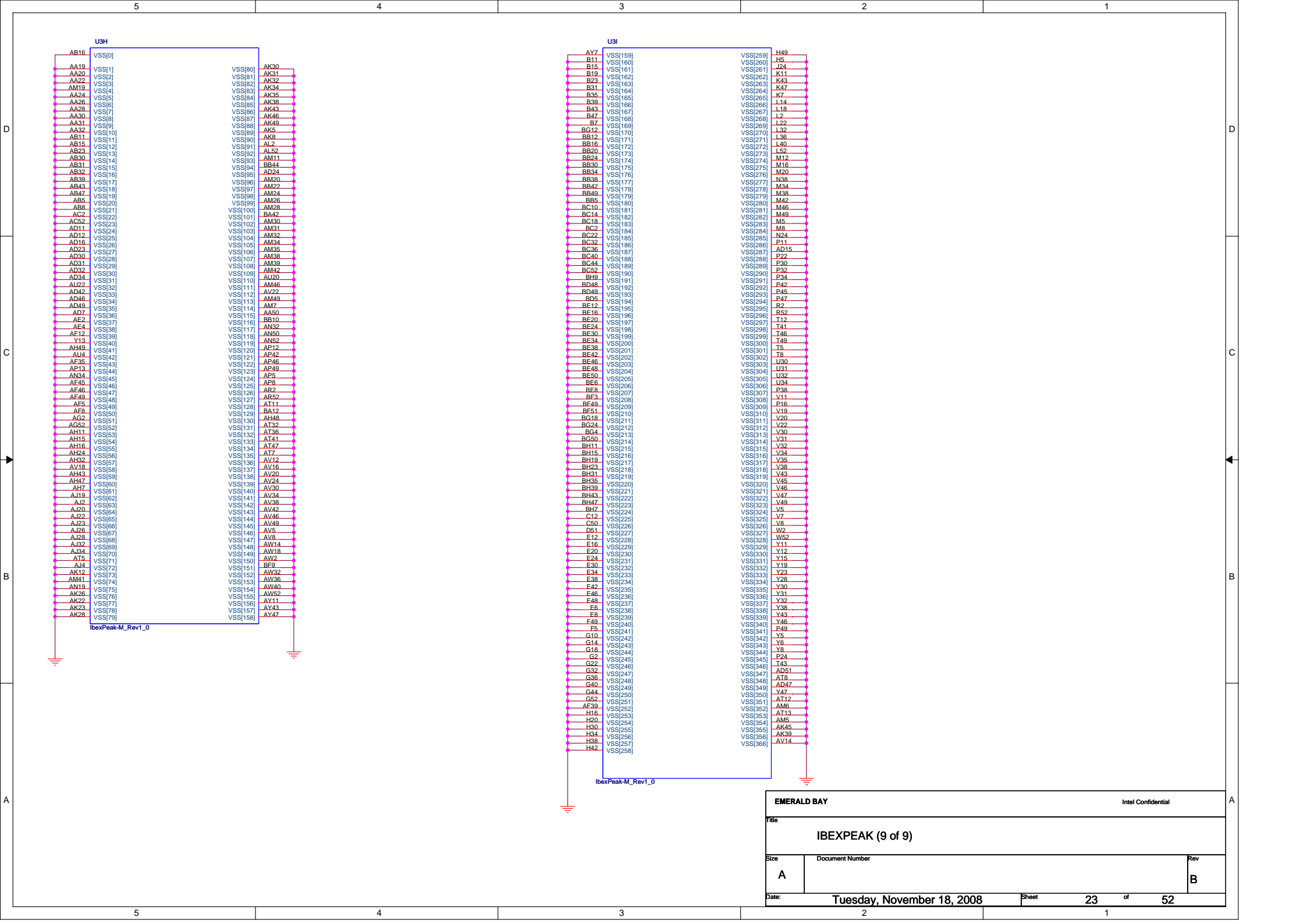




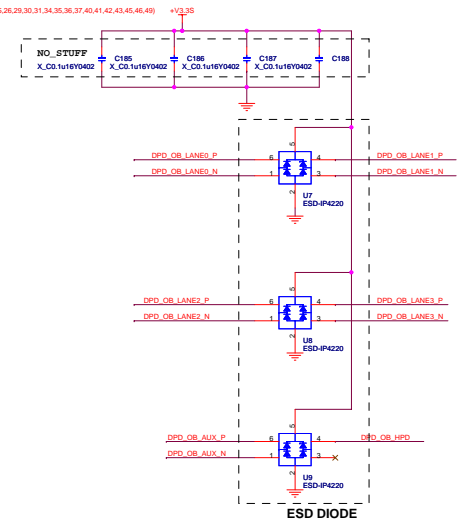
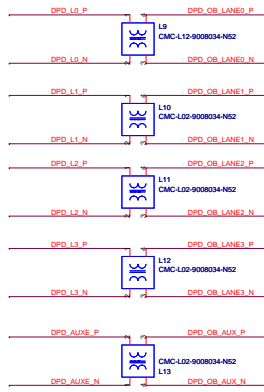
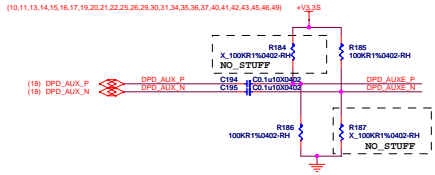




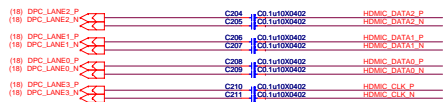
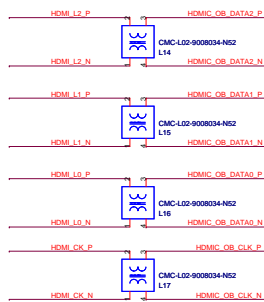
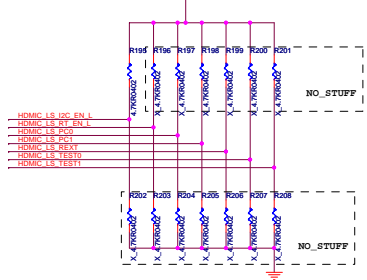
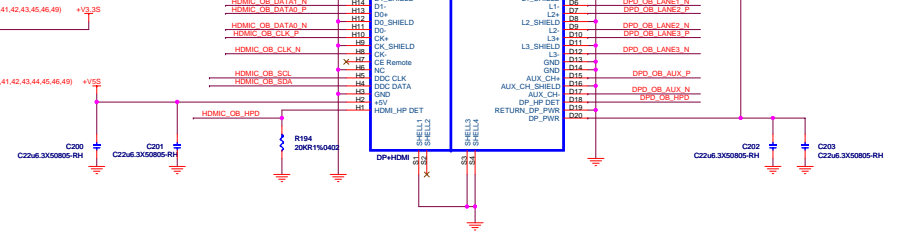
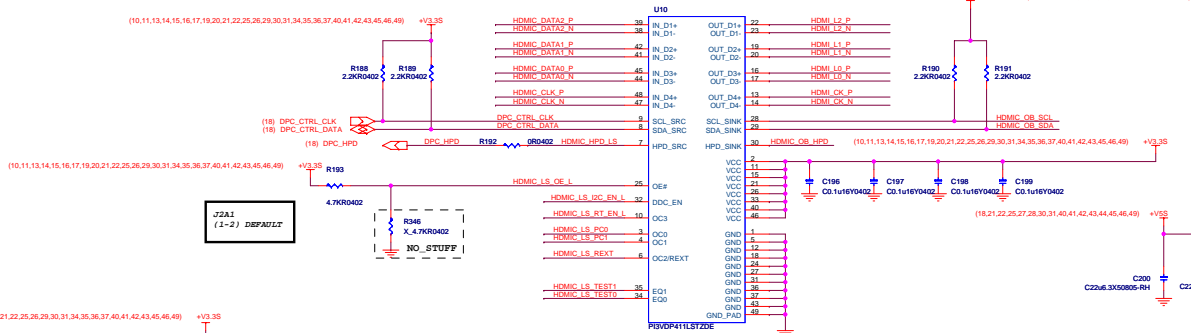




DISPLAY PORT

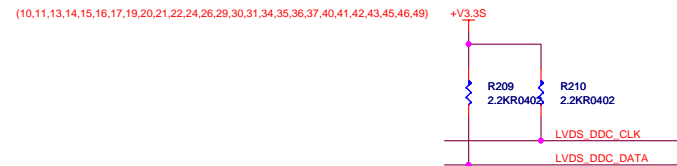
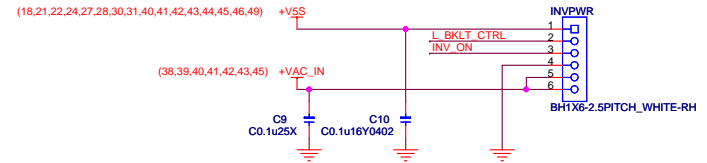
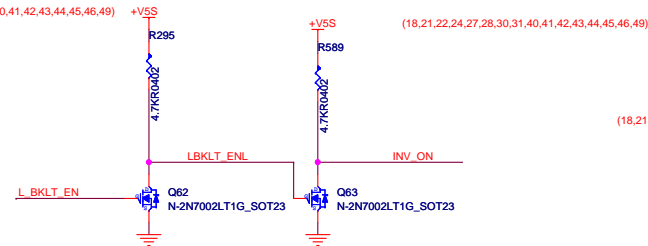
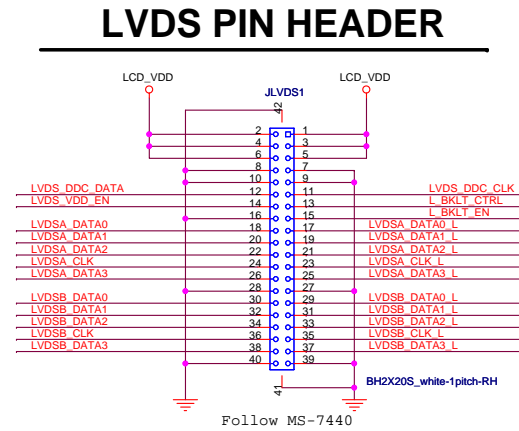
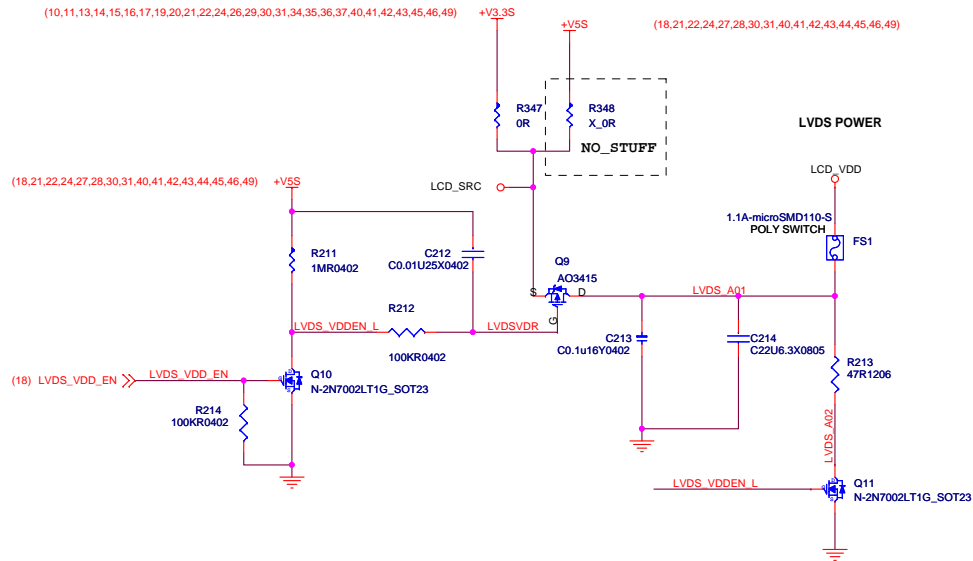
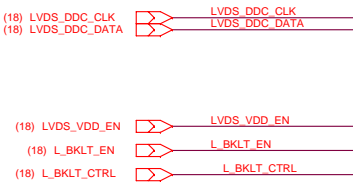
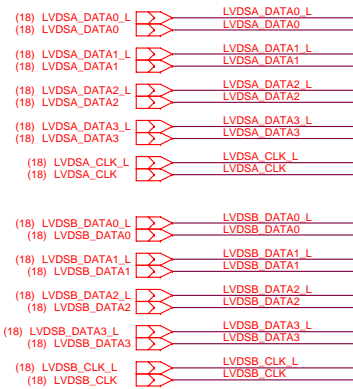


HDMI LEVEL SHIFTER

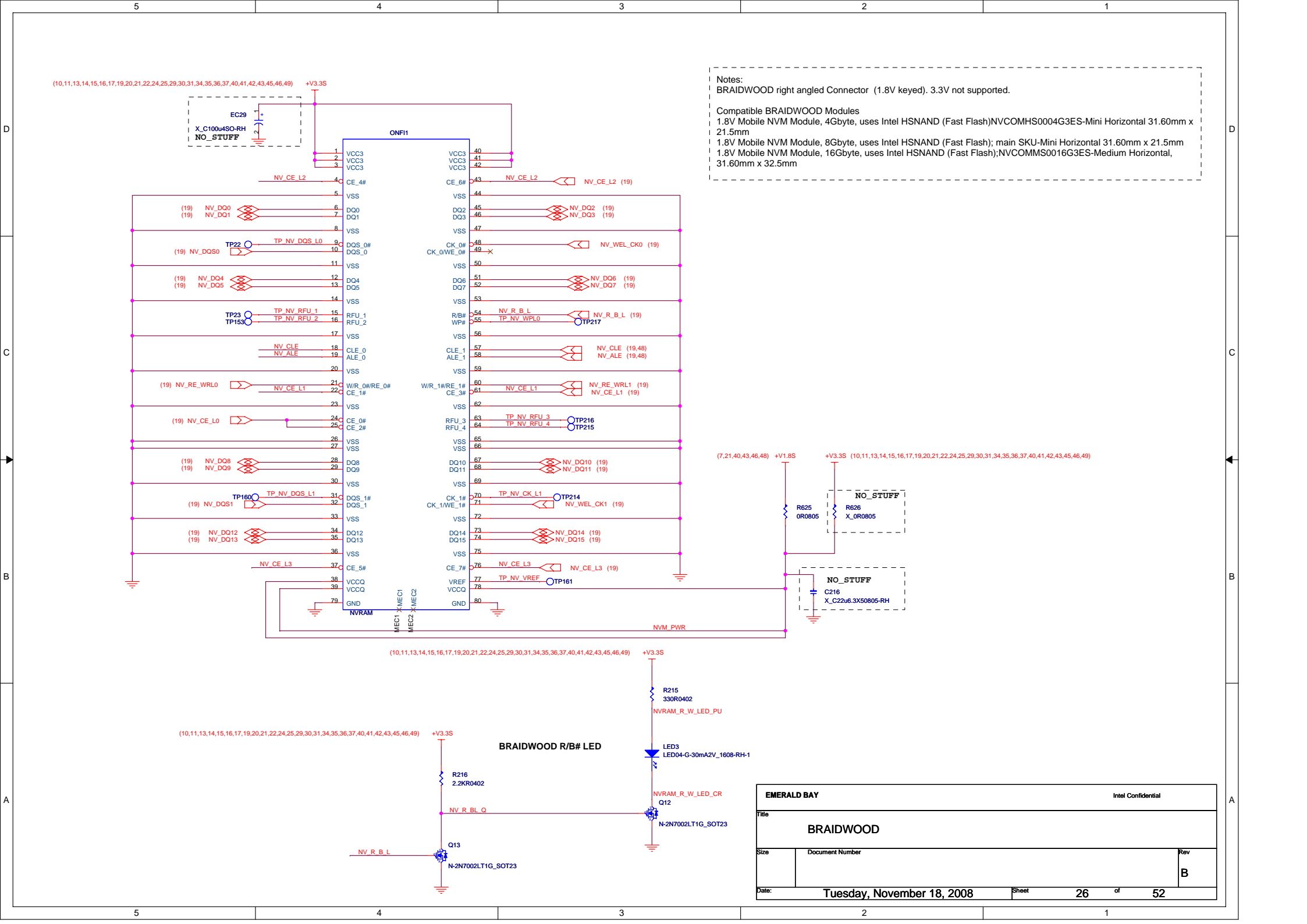


EMERALD BAY		Initial Confidential	
File			
DISPLAY PORT			
Doc B		Document Number	
Date Tuesday, November 18, 2008		Rev B	
Sheet		24 of 52	

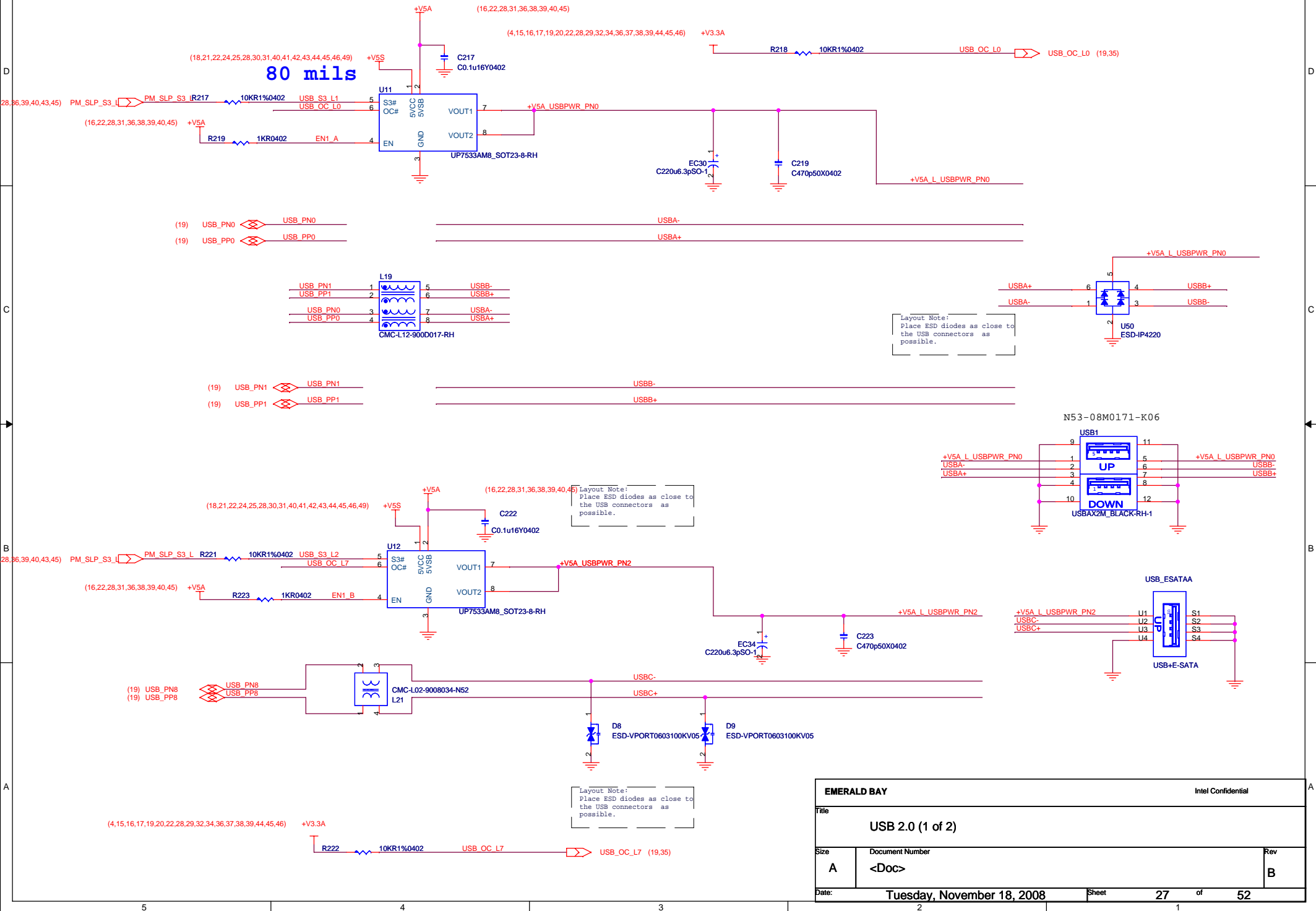
Note:
MSI to add LVDS connector and circuitry



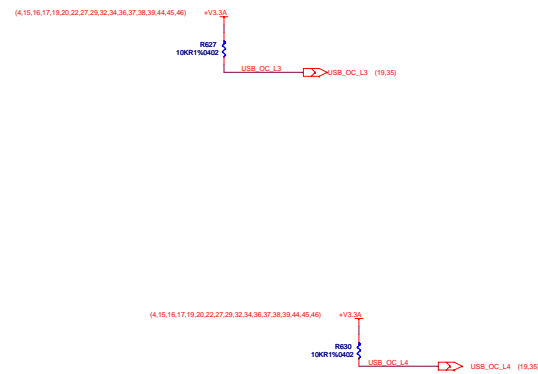
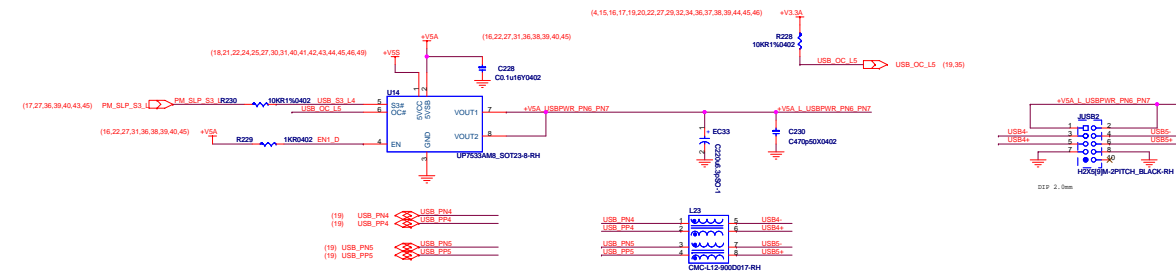
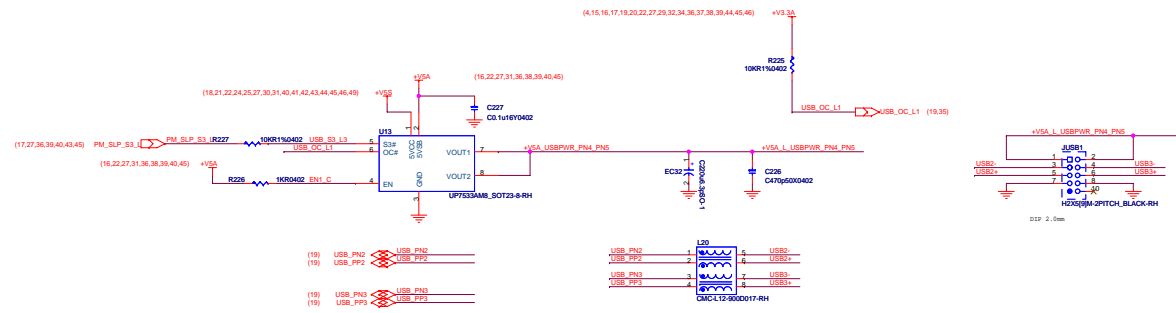
EMERALD BAY		Intel Confidential	
Title			
LVDS			
Size	Document Number		Rev
A			B
Date:	Tuesday, November 18, 2008	Sheet	25 of 52



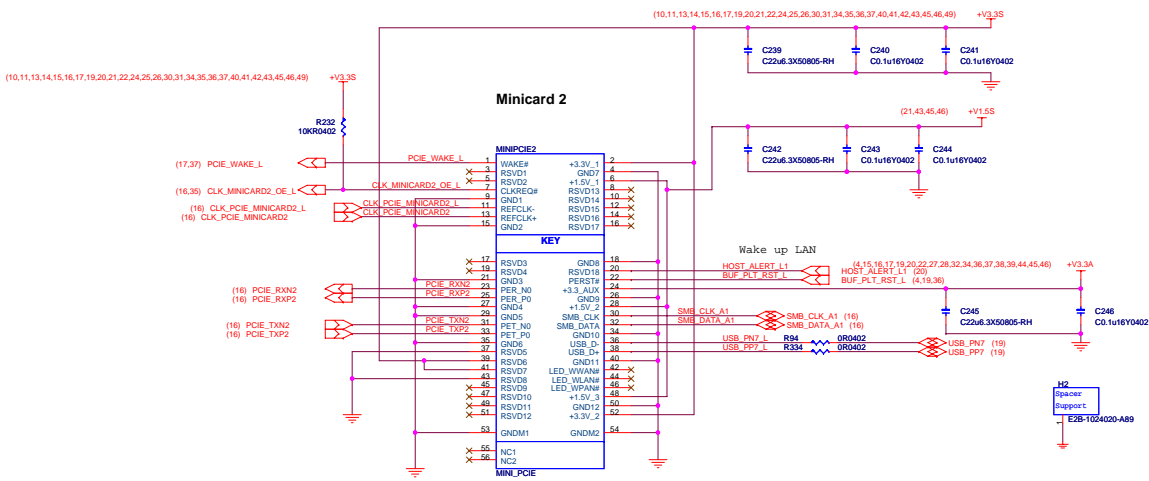
USB PORTS: 0,1,2



USB PORTS: 4,5,6,7

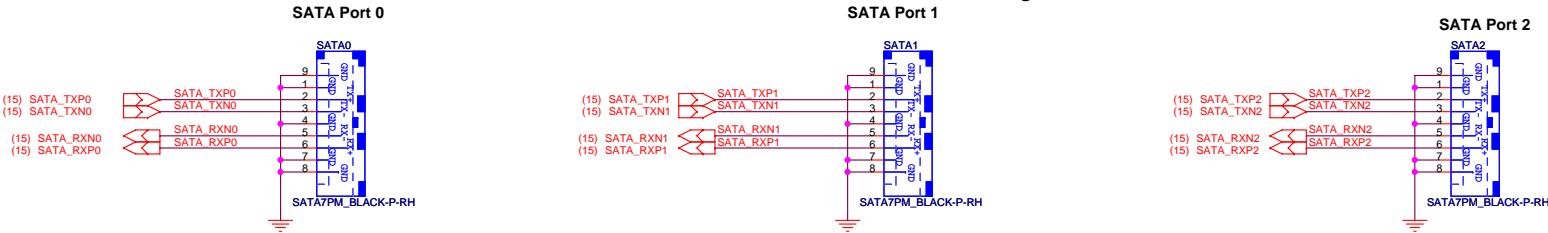


mini-PCIE H:4.85 mm BOTTOM

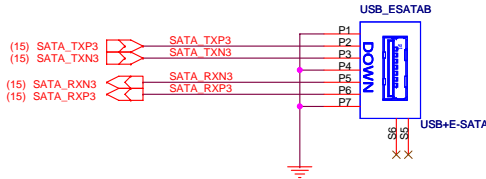


SATA PORTS (0,1, 2, and 3)

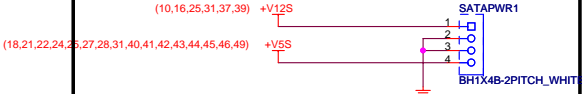
SATA Signal Connectors



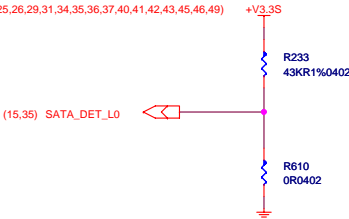
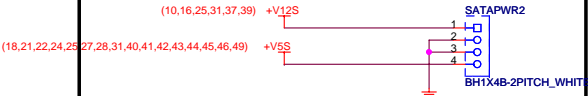
e-SATA



FOR SATA POWER CONN



FOR SATA POWER CONN

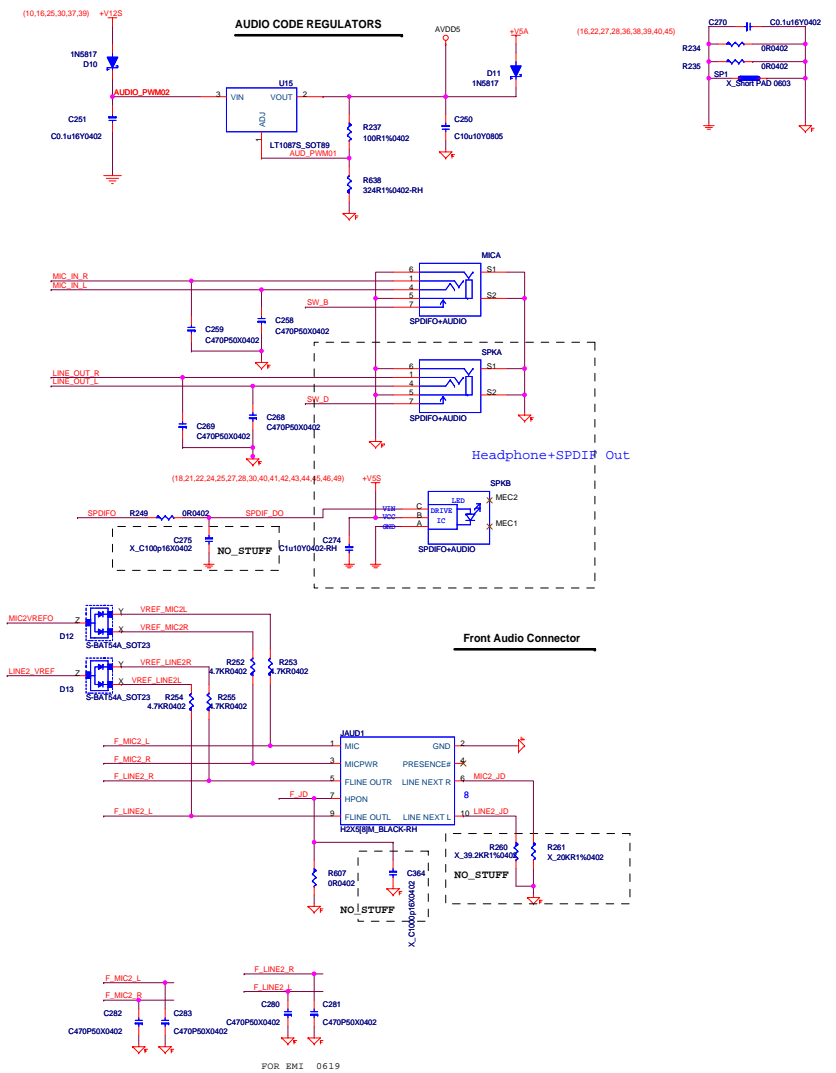
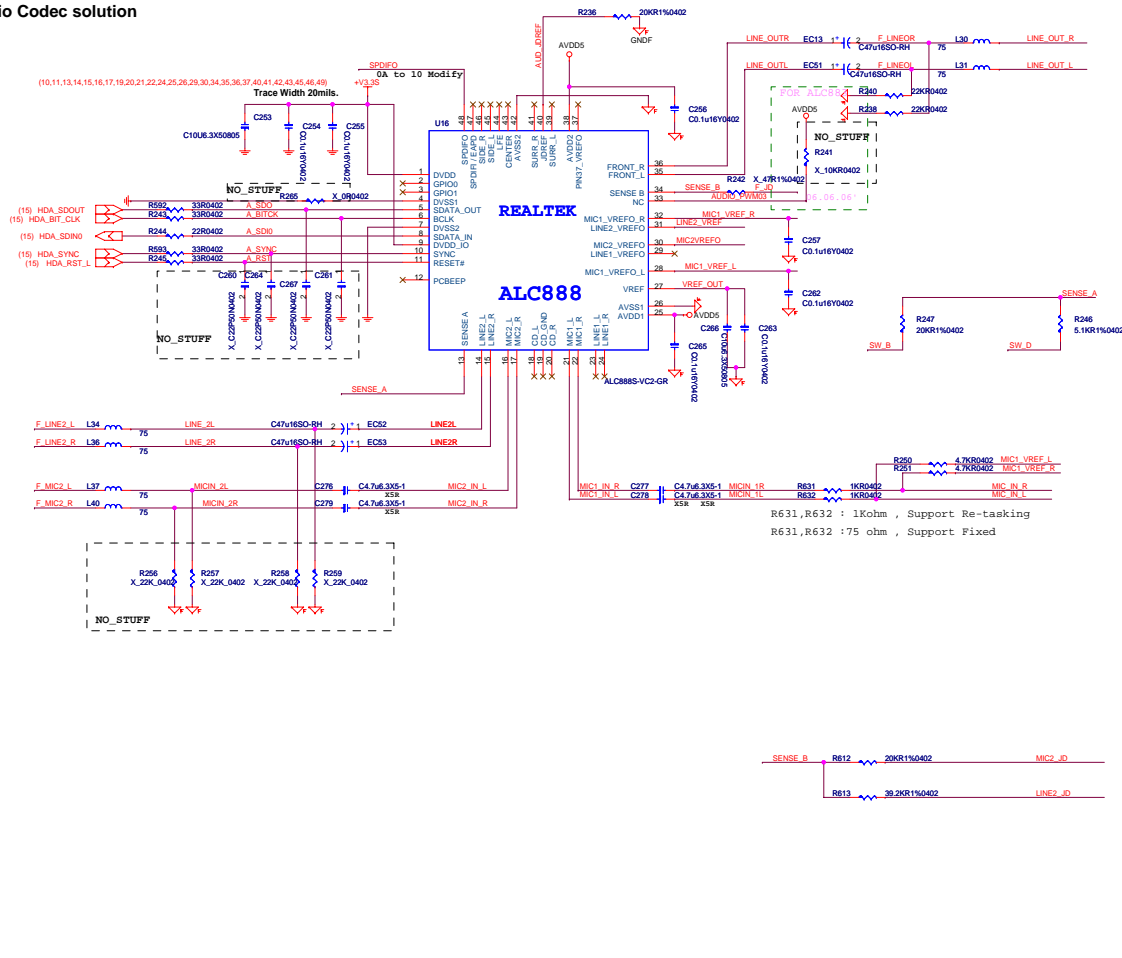


This jumper simulates the drive status. For proper function of the hot plug, this jumper must be "No Shunt" when drive is removed and "Shunt" after the drive is plugged in.

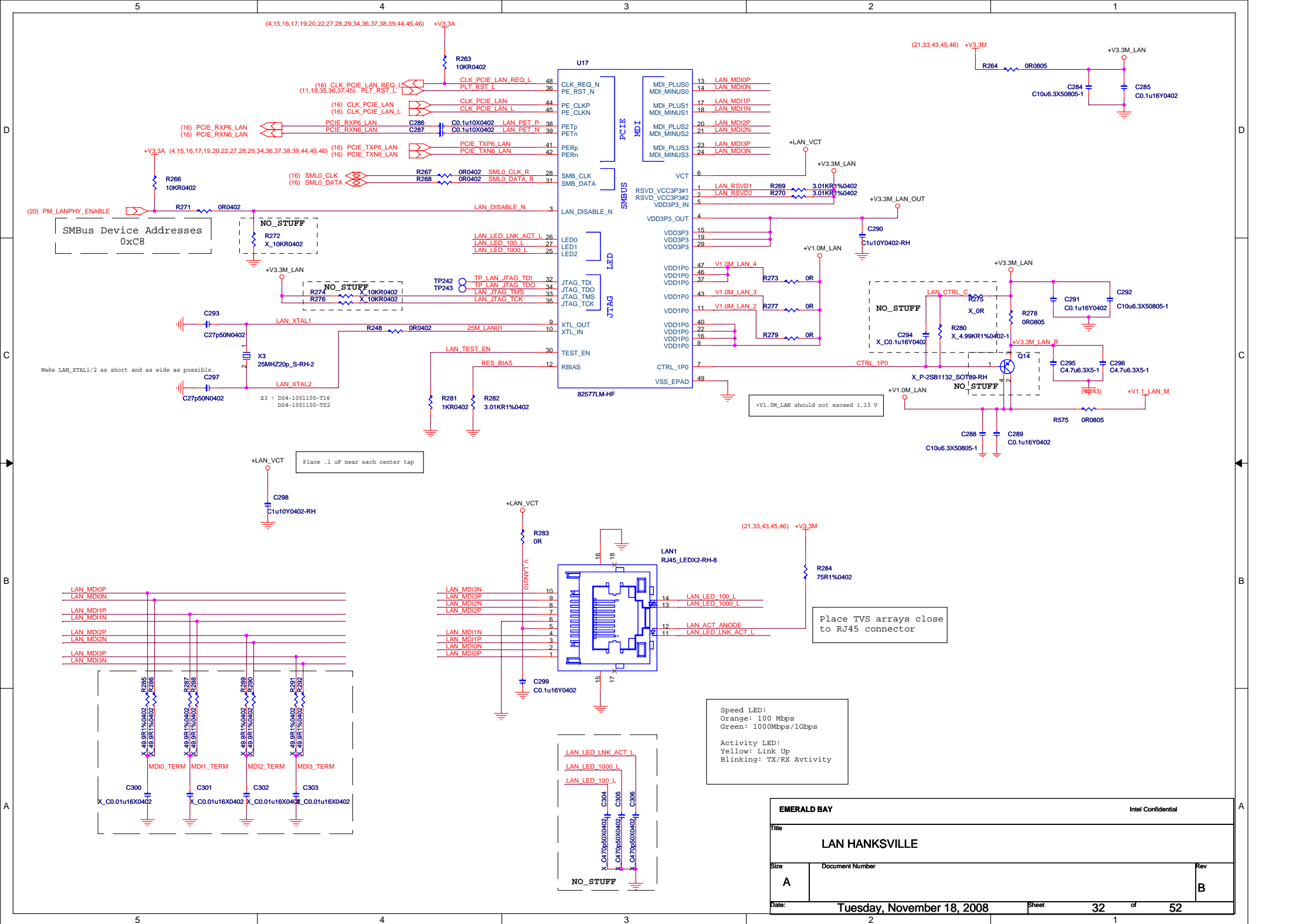
EMERALD BAY		Intel Confidential	
Title			
SATA			
Size	Document Number		Rev
	<Doc>		B
Date:	Tuesday, November 18, 2008	Sheet 30 of 52	

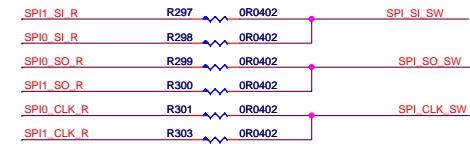
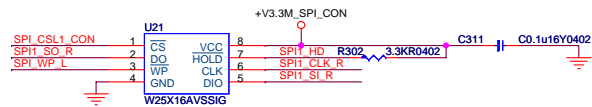
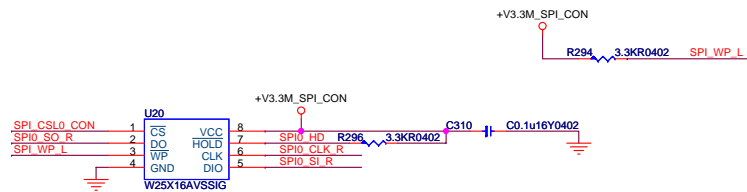
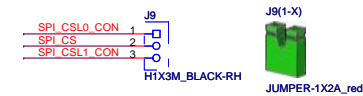
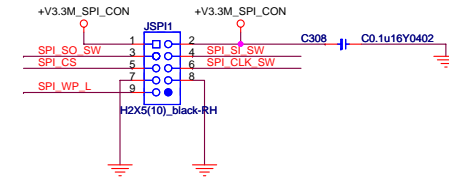
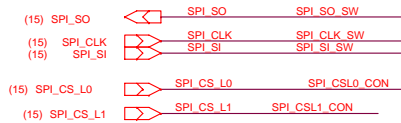
Realtek ALC888 CODEC

NOTE:
MSI to add Audio Codec solution

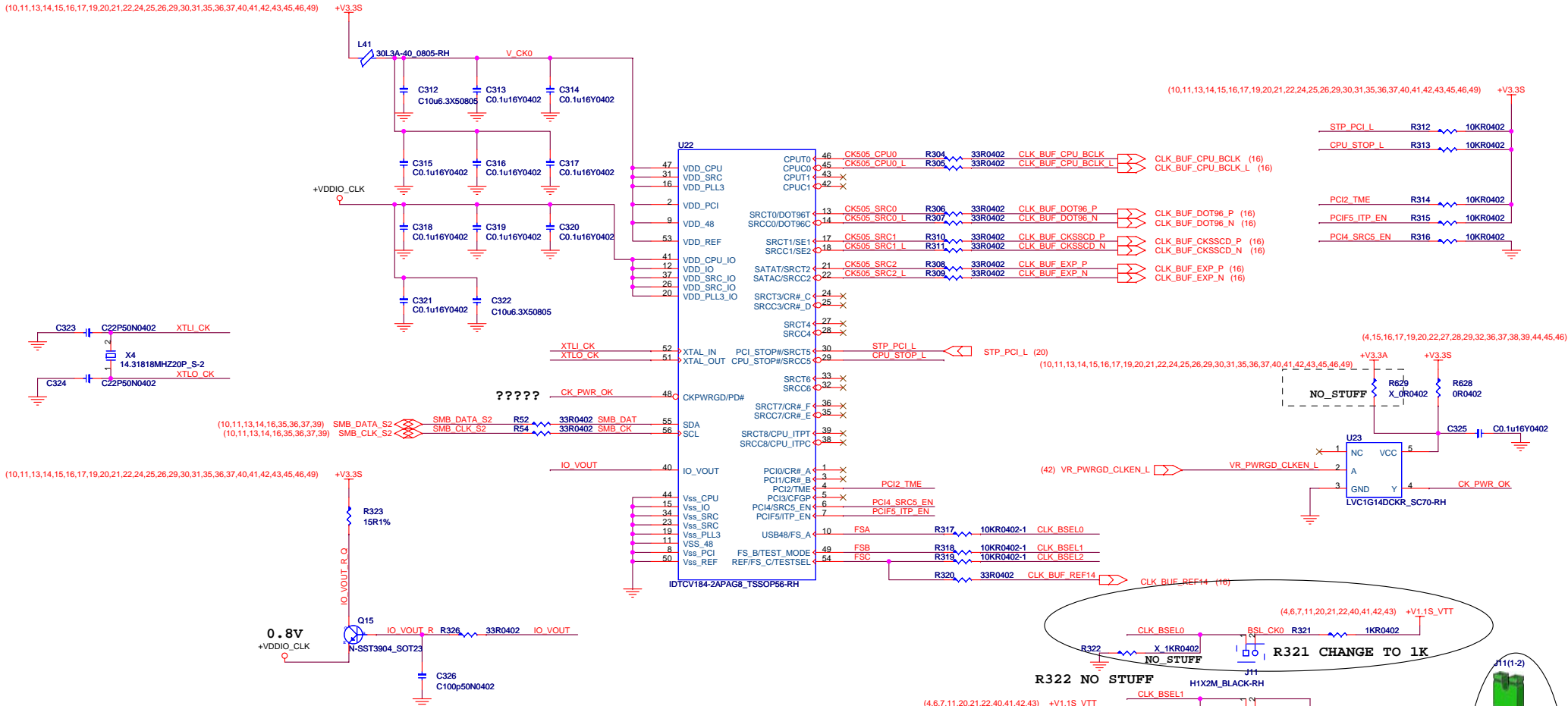


EMERALD BAY		Intel Confidential	
File IHDA			
Size B	Document Number		Rev B
Date:	Tuesday, November 18, 2008	Sheet 31	of 52





EMERALD BAY		Intel Confidential	
Title			
SPI			
Size	Document Number		Rev
A			B
Date:	Tuesday, November 18, 2008	Sheet	33 of 52



54	REF/FS_C/TestSel	I/O	14.318MHz. Frequency Select at CKPWRGD assertion. Selects test mode if pulled above 2V at CKPWRGD assertion.
48	CKPWRGD/PD#	IN	CKPWRGD power good, active LOW, used to latch FSA,B,C,I,TP_EN, TME, and SRC5_EN, active HIGH. After, becomes power down, LOW active.

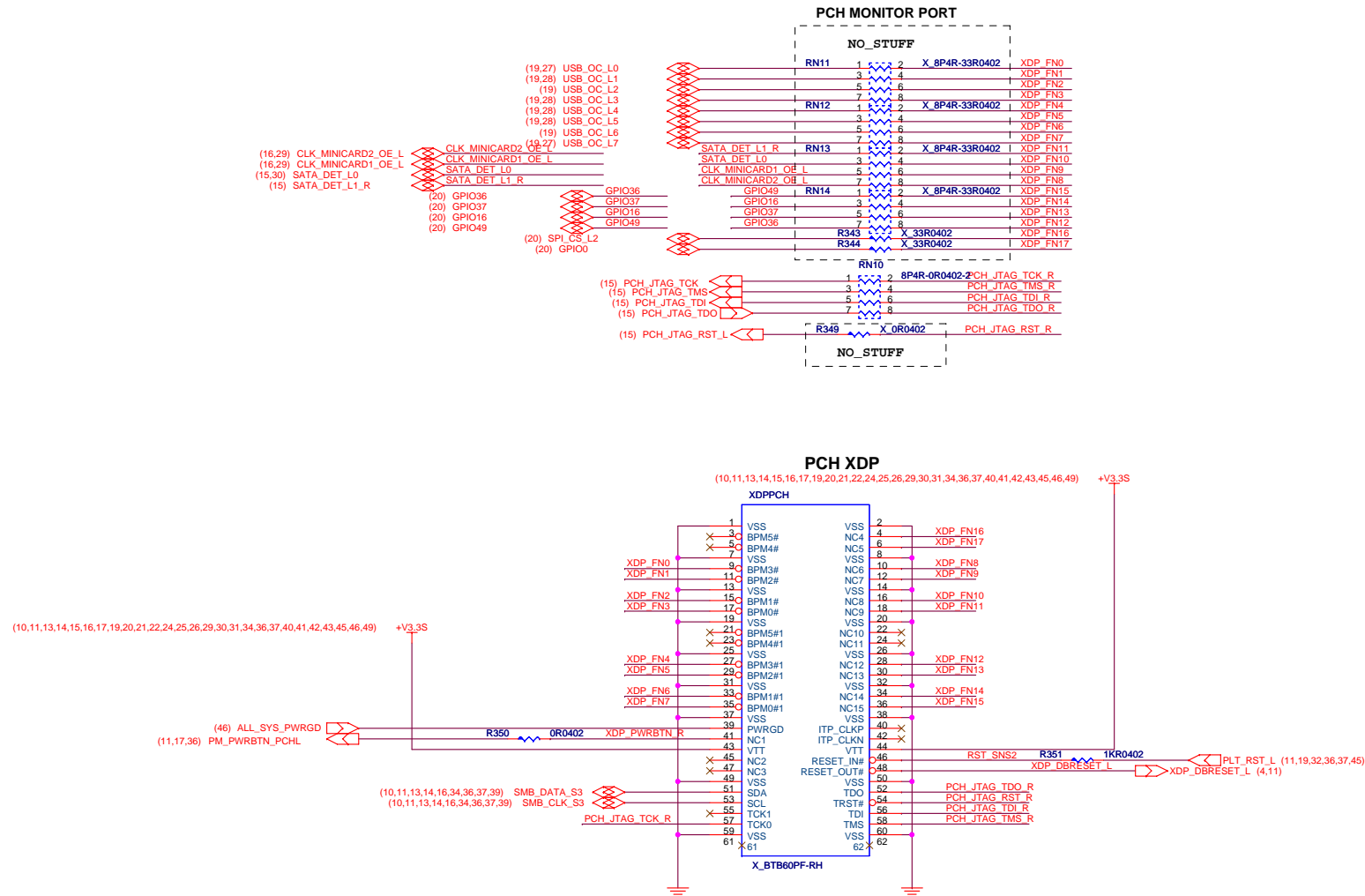
FREQUENCY SELECTION

FSC, B, A	CPU	SRC[7:0]	PCI	USB	DOT	REF
101	100	100	33.3	48	96	14.318
001	133	100	33.3	48	96	14.318
011	166	100	33.3	48	96	14.318
010	200	100	33.3	48	96	14.318
000	266	100	33.3	48	96	14.318
100	333	100	33.3	48	96	14.318
110	400	100	33.3	48	96	14.318
111	Reserve	100	33.3	48	96	14.318

BCLK Frequency Select:	
133 MHz DEFAULT	J11 -> 1-2 J12 -> 1-2 J13 -> 1-2

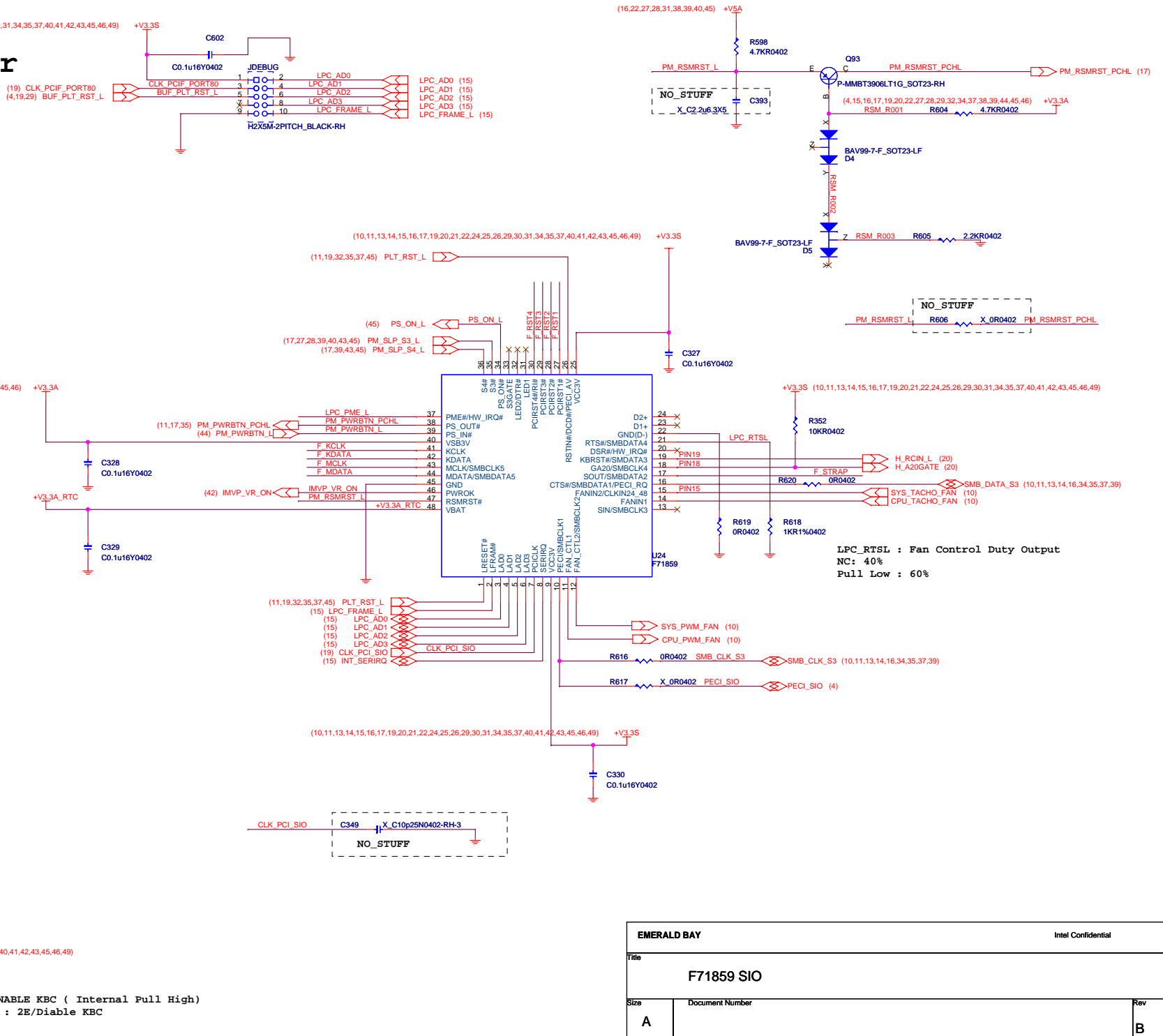
EMERALD BAY		Intel Confidential
Title CK 505		
Size A	Document Number	Rev B
Date: Tuesday, November 18, 2008	Sheet 34	of 52

IBEXPEAK DEBUG



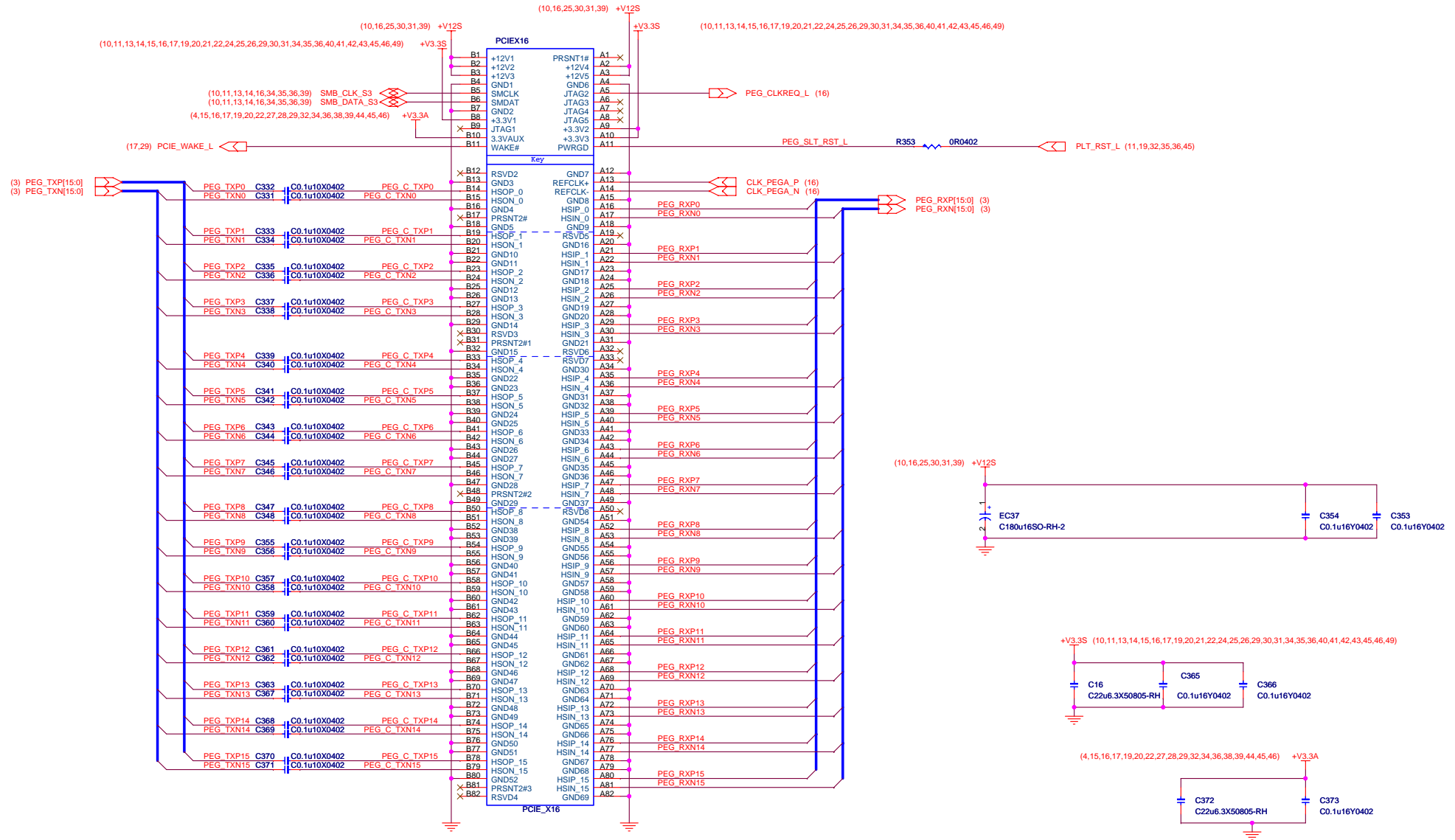
EMERALD BAY		Intel Confidential	
Title			
IBEXPEAK-M XDP			
Size	Document Number		Rev
A			B
Date:	Tuesday, November 18, 2008	Sheet 35 of 52	

Port80 header



EMERALD BAY		Intel Confidential	
Title			
F71859 SIO			
Size	Document Number		Rev
A			B
Date:	Tuesday, November 18, 2008	Sheet	36 of 52

PEG



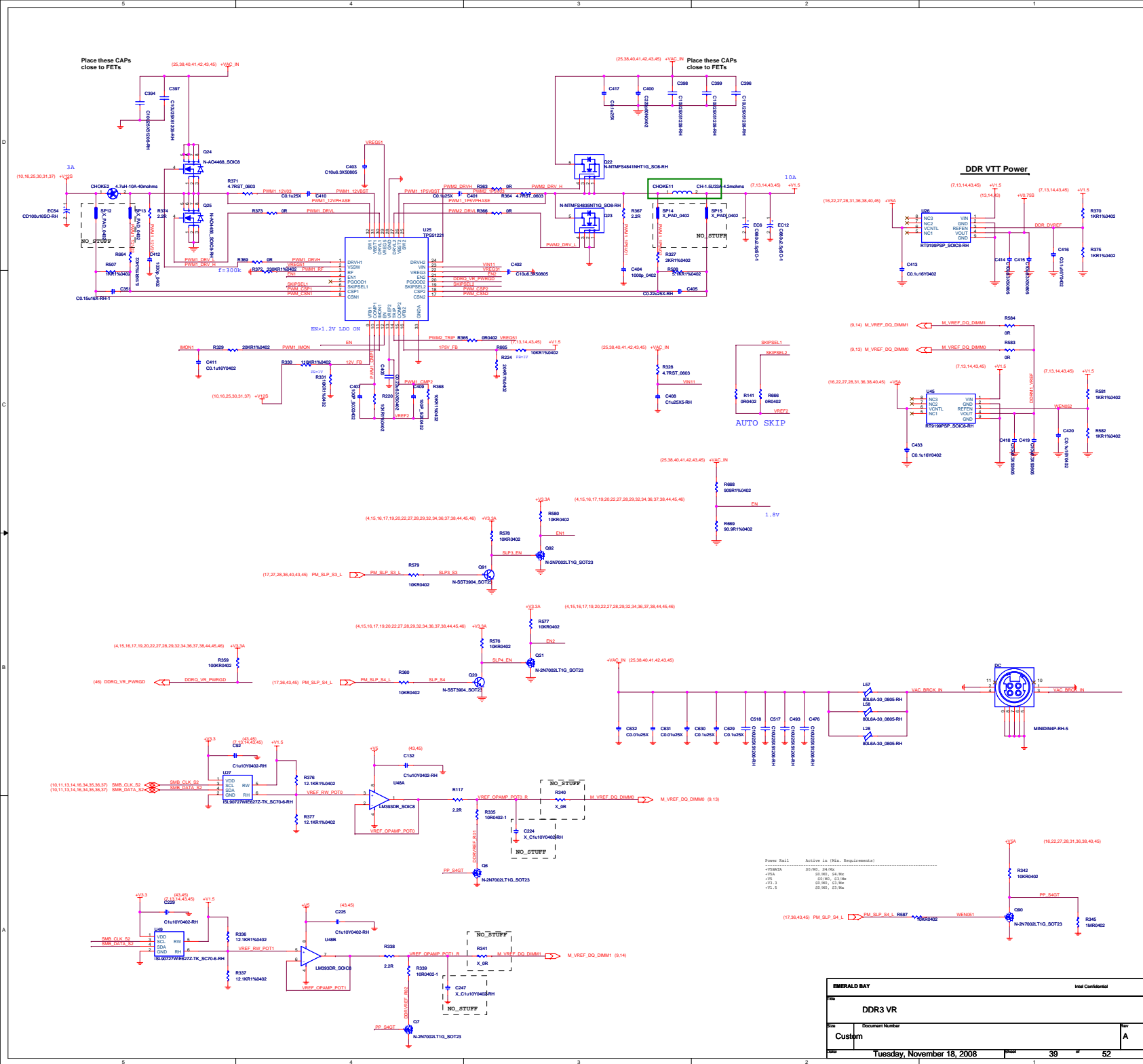
EMERALD BAY		Intel Confidential	
Title			
PCIe x16			
Size	Document Number		Rev
A			B
Date:	Tuesday, November 18, 2008	Sheet	37 of 52

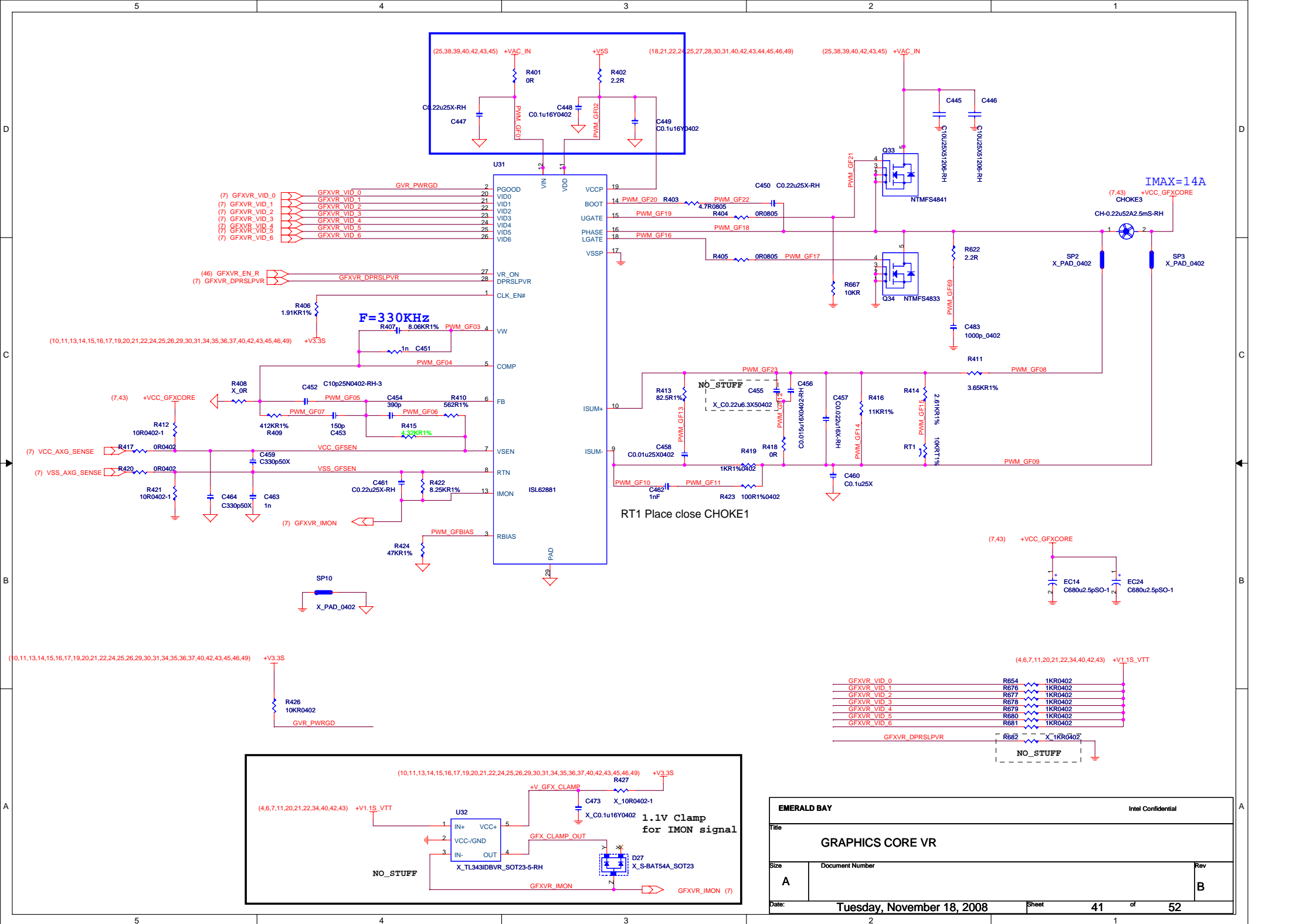
Imax=8A OCP=10

+5V_{SUS}

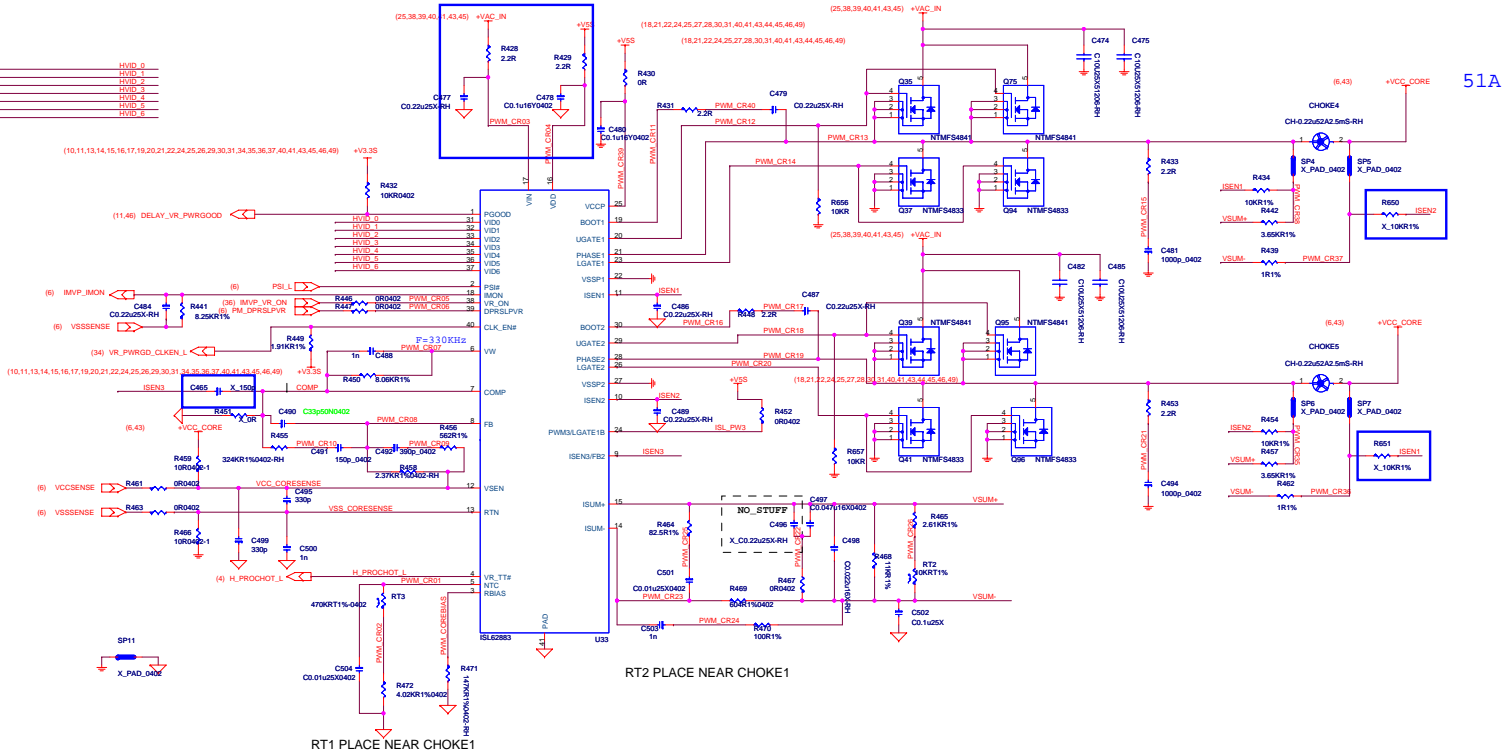
Imax=8A OCP=10

EMERALD BAY		Intel Confidential	
Doc			
TPS51125 SYSTEM POWER VR			
Doc		Document Number	
Custom		Rev	
Date:		Tuesday, November 18, 2008	
Sheet		38 of 52	

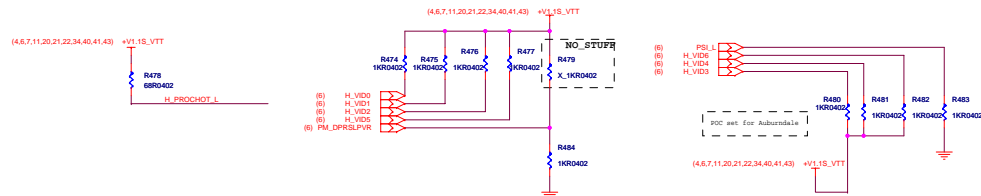




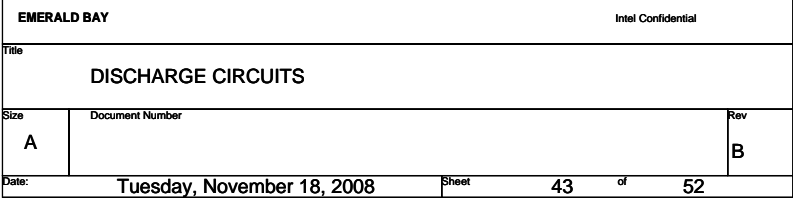
(6) H_VDD0
(6) H_VDD1
(6) H_VDD2
(6) H_VDD3
(6) H_VDD4
(6) H_VDD5
(6) H_VDD6
(6) H_VDD7

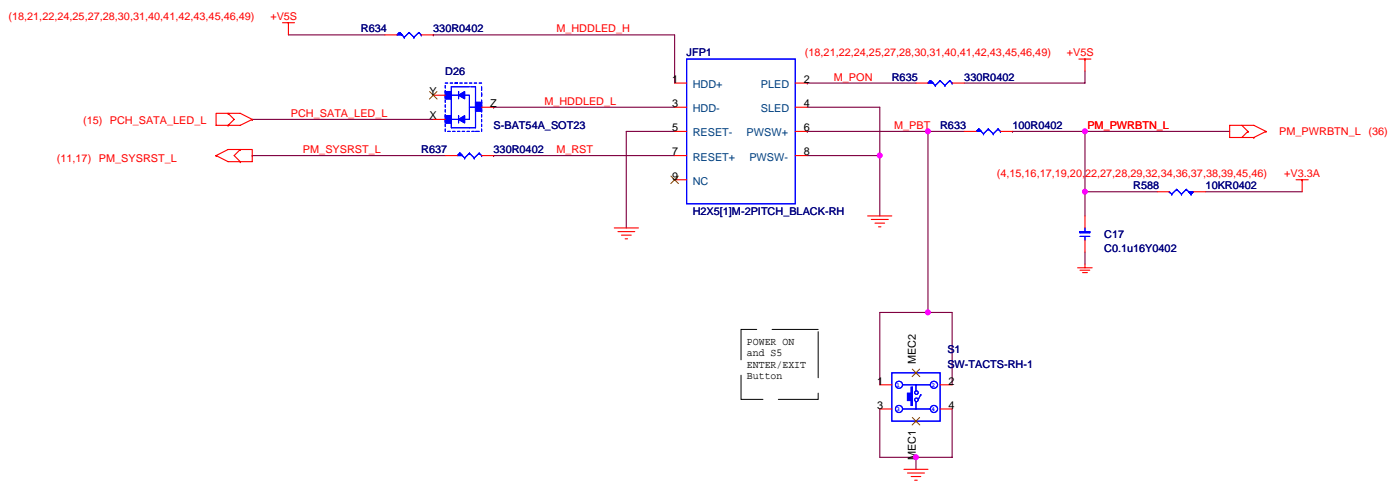


51A

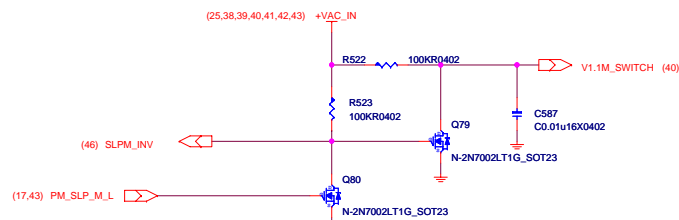
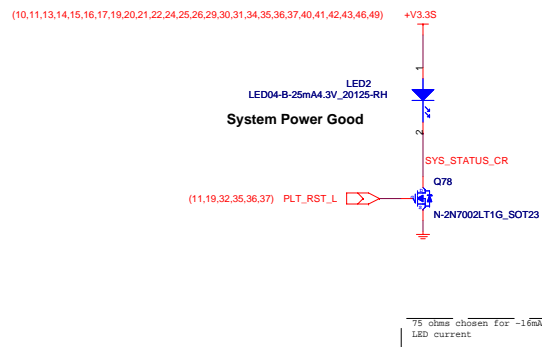
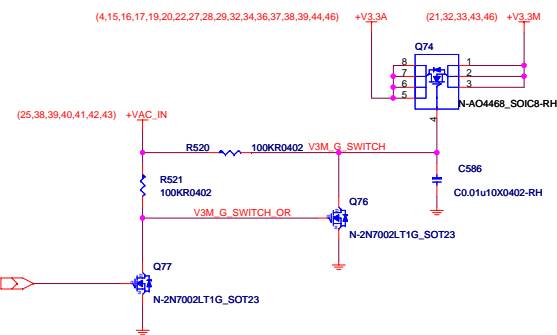
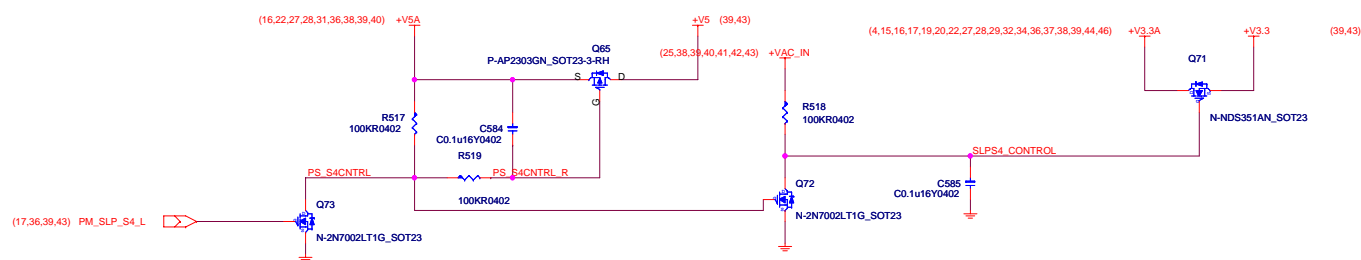
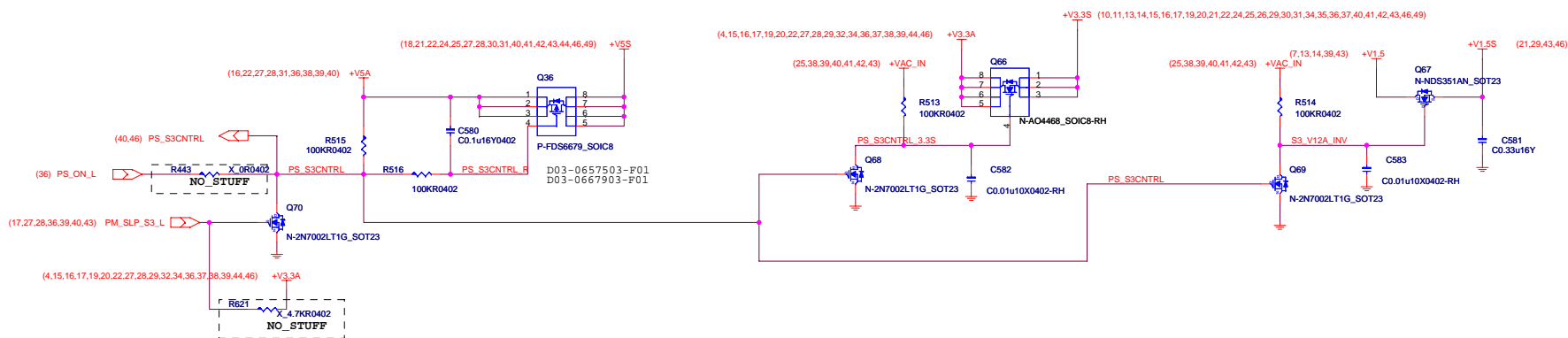


EMERALD BAY		Intel Confidential	
File		IMVP-6.5	
Size	Document Number	Rev	
B		B	
Date	Tuesday, November 18, 2008		42 of 52



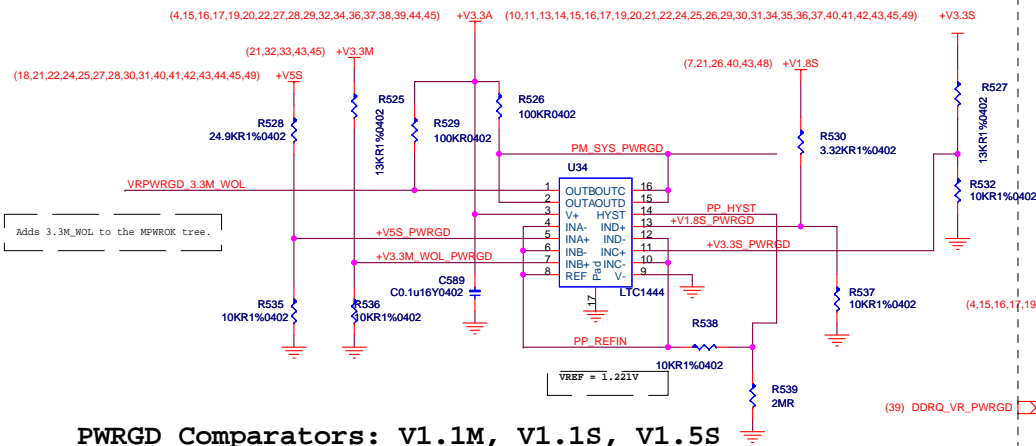


EMERALD BAY		Intel Confidential	
Title			
START UP SEQUENCE			
Size	Document Number		Rev
A			B
Date:	Tuesday, November 18, 2008	Sheet	44 of 52

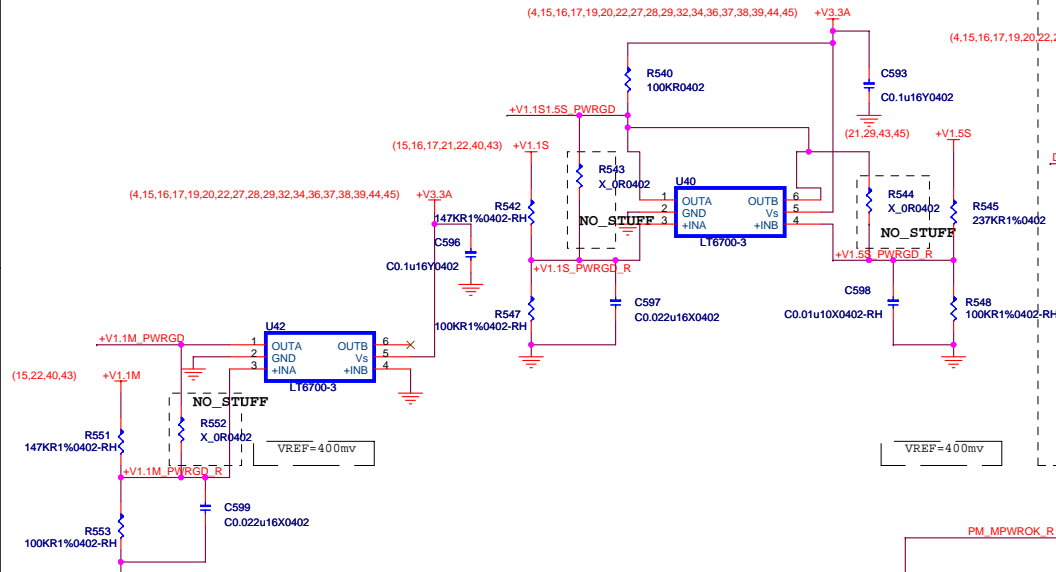


EMERALD BAY		Intel Confidential	
Title			
SLEEP CONTROL			
Size	Document Number		Rev
Custom			B
Date:	Tuesday, November 18, 2008	Sheet	45 of 52

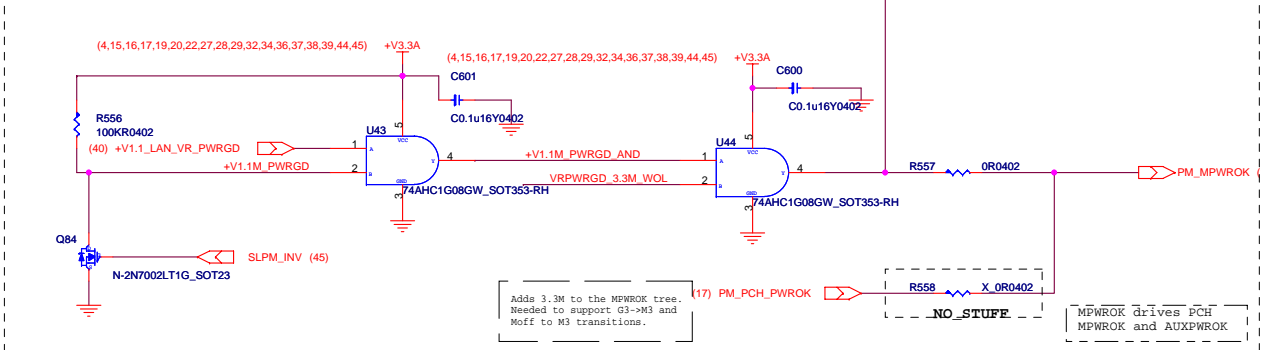
PWRGD Comparators: V5S, V3.3S, V3.3M, V1.8S



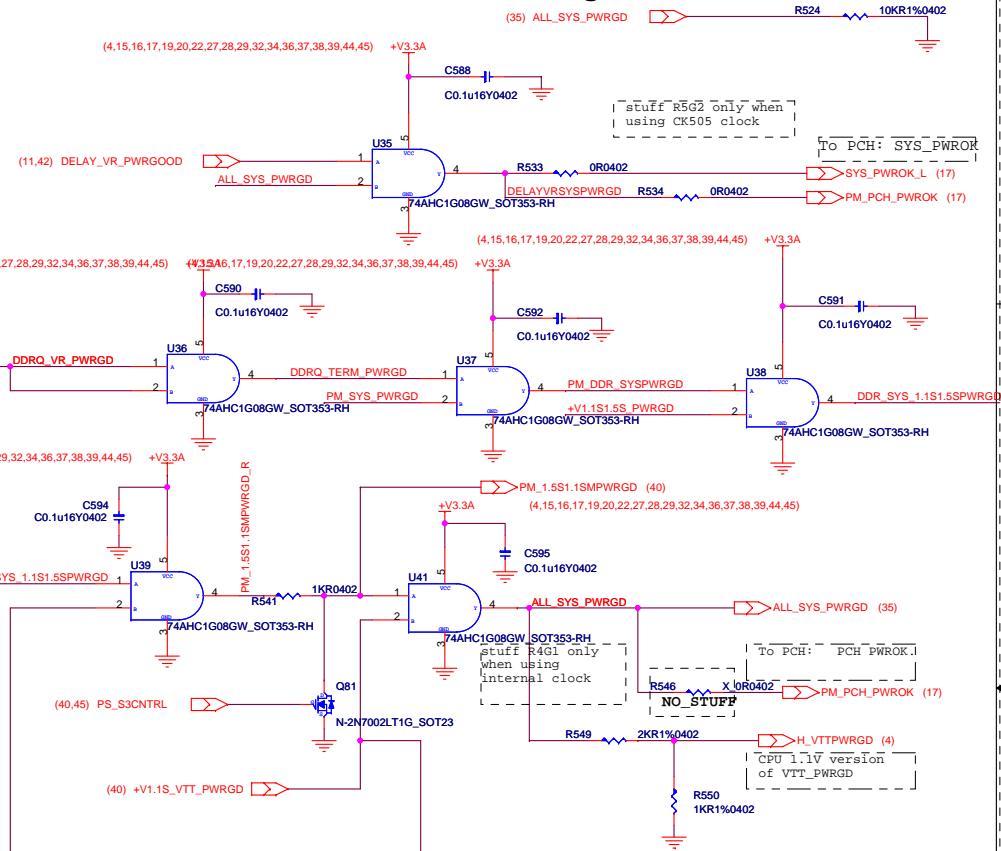
PWRGD Comparators: V1.1M, V1.1S, V1.5S



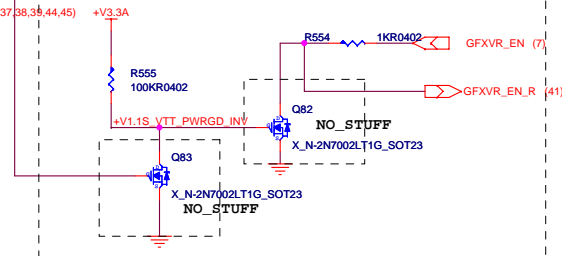
iAMT PWROK Logic



Main S0 PWROK Logic



Optional Gfx VR_EN Delay



EMERALD BAY

Intel Confidential

POWER SEQUENCE LOGIC

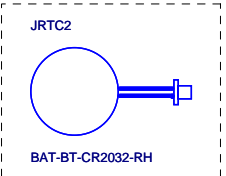
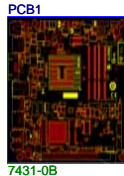
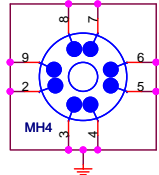
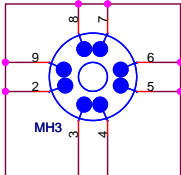
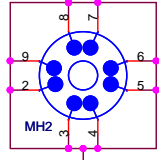
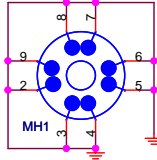
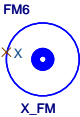
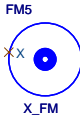
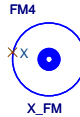
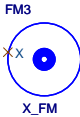
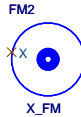
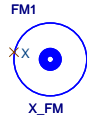
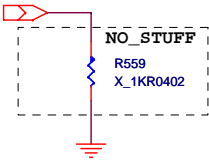
Size	Document Number	Rev
A		B
Date:	Tuesday, November 18, 2008	Sheet 46 of 52

Note: ** means non_IAMT system

A

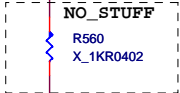
HW Strap Purpose	PCH Pin
No Reboot	SPKR
RSVD	GPIO[34]
Al6 swap override	GNT[3]#/ GPIO[55]
Integrated VRM Enable/Disable	INTVRMEN
Boot BIOS Strap bit [1] BBS[1]	GNT[1]#/ GPIO[51]
Boot BIOS Strap bit[0] BBS[0]	GNT[0]#
ESI Strap (Server only)	GNT[2]#/ GPIO[53]
Intel Anti-Theft Technology Enable	NV_ALE
Flash Descriptor Security Override	GPIO33/DOCK_EN#
TPM Functionality Disable	SPI_MOSI
DMI Termination Voltage	NV_CLE
RSVD	HDA_SDO
RSVD	GPIO[8]
RSVD	GPIO[27]
RSVD	HDA_SYNC
RSVD	GPIO[15]

ESI Strap (Server only)	
PCH_GPIO53	Low = Enabled
	High = Disabled



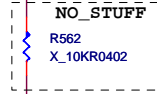
RTC Battery

DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW
	Set to Vcc/2 when HIGH



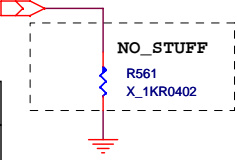
(19,26) NV_CLE

Intel Anti-Theft Technology Enable	
NV_ALE	High = Enabled Stuff PU
	Low = Disabled Unstuff PU (Default)

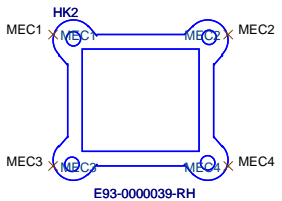
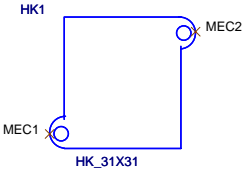


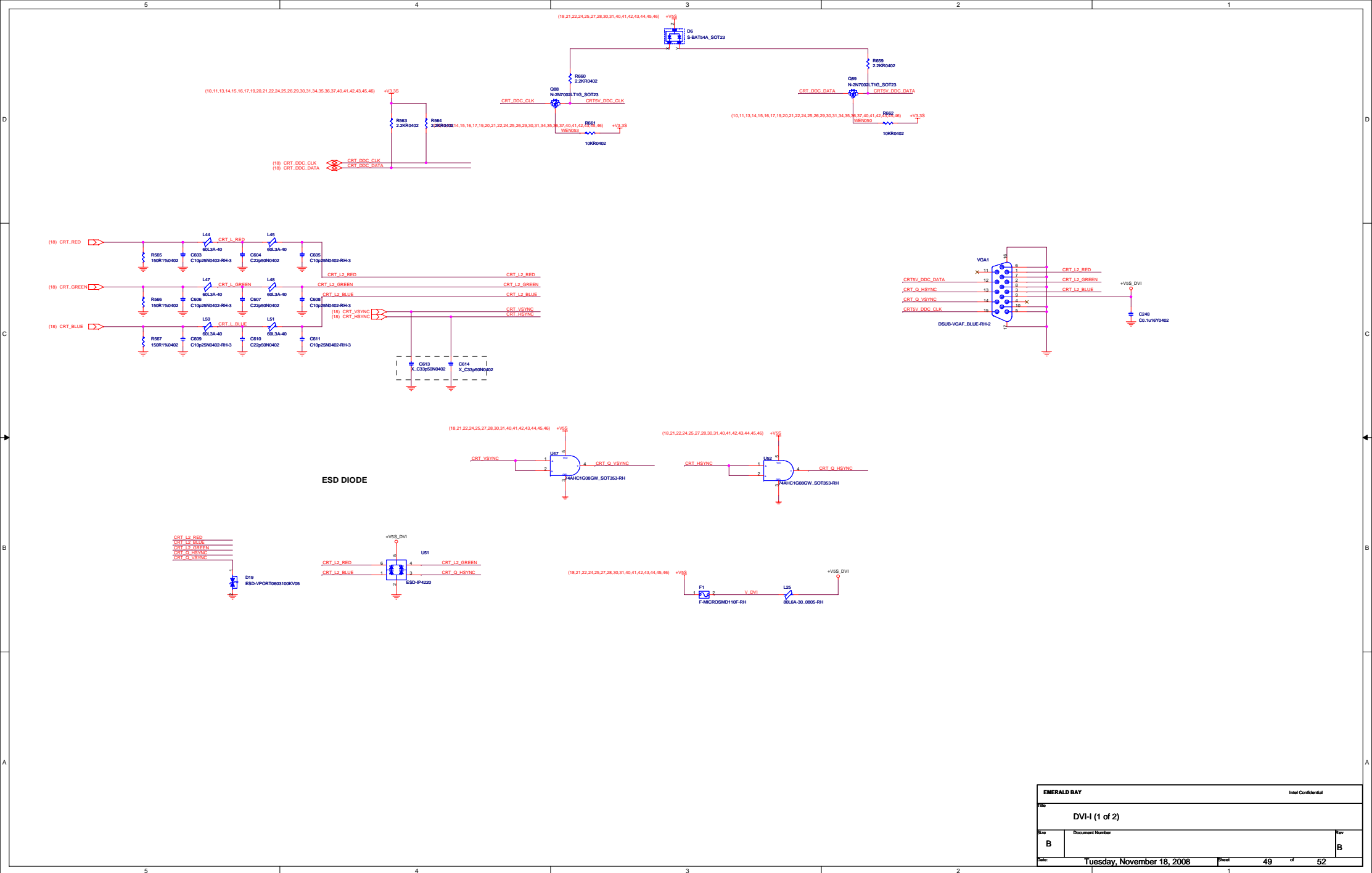
(19,26) NV_ALE

Al6 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = Al6 swap override/Top-Block Swap Override enabled
	High = Default



(19) PCL_GNT_L3





A

	5	4	3	2	1																																				
D	07-30-08 03.Page 45 :Add Pin Header 2x5 Pin for Power On , HDD LED , Reset Function---- From MSI System 04.Page 20 :Add GPIO49 Pull-High 10Kohm 0402 to +V3.3S 05.Page 49 :Add PCB impedance coupon trace 06.Page 30 :Add J18 SATA Power Connector 07-31-08 01.Page 36 : Add +V3.3A_RTC Voltage connect to U24 Pin 48 ---- From Fintek System 02.Page 39 : Change CN6 for 11A DC Jack 03.Page 27,28 : U11,U12,U13,U14,U48,U49 From TPS2052B Change to UP7533 04.Page 27 : CN3 From USBx3 Vertical Change to Dual USB Port 05.Page 27,30 : Add USB Port + E-SATA -- CN4 06.Page 10 : Add DC FAN and PWM FAN Co-Lay 07.Page 40 : +VAC_IN of Q26 add a Cap : C569 --- From Power Suggestion 08.Page 40 :+V1.1S needs to delay , add C71 0.1uF --- From Demo design Suggestion 09.Page 40 :+V1.8S needs a control signal by PM_SLP_S3# --- From Power Sequence REV:0.71 Suggestion 10.Page 39 : --- Q22 From AO4458 change NTMFS4841NHT1G , Q23 From AO4458 change NTMFS4835NT1G ----Fromm Power Suggestion 11.Page 38 :Net Name : +V5A add a Cap. EC47 220uF/6.3V --- From Power Suggestion 12.Page 38 :Net Name : +V3.3A add a Cap. EC31220uF/6.3V --- From Power Suggestion 13.Page 38 : PUL Pin 14 add resistor(R652 and R653) for Freq. Selection --- From Power Suggestion 14.Page 38 : Net name : VR_ALN_ENABLE add a resistor R654 20K to GND --- From Power Suggestion 15.Page 42 : Add R655 2,2 ohm , C570 1000PF --- From Power Suggestion 16.Page 42 : C490 from 10PF change 33PF , R458 from 2.87K ohm change 2.49K ohm --- From Power Suggestion 17.Page 42 : C496 from 0.33uF change 0.22uF , C497 from 27nF ohm change 47nF , R469 from 1.5K ohm change 806 ohm--- From Power Suggestion 18.Page 42 :Net Name :ISEN3 add C571 0.22uF to GND --- From Power Suggestion 19.Page 42 :LGATE MOSFET add a puul-down 10Kohm to GND on Pin G --- From Power Suggestion 08-01-08 01.Page 15 : Net Name :PCH_JTAG_TMS add R640 51 ohm pull-high to +V1.1M--- From Intel Suggestion 02.Page 15 : Net Name :PCH_JTAG_TDI add R641 51 ohm pull-high to +V1.1M--- From Intel Suggestion 03.Page 15 : Net Name :PCH_JTAG_TDO add R642 51 ohm pull-high to +V1.1M--- From Intel Suggestion 04.Page 15 : Net Name :PCH_JTAG_RST# add R643 10K ohm pull-high to +V1.1M and add R644(no stuff) pull-down to GND--- From Intel Suggestion 05.Page 15 : Net Name :PCH_JTAG_TCK add R645 4.75K ohm 1k pull-down to GND-- From Intel Suggestion 08-05-08 01.Page 51 : Net Name :CRT_DDC_CLK and CRT_DDC_DATA add level shift circuit--- From Intel Suggestion 02.Page 09 : Net Name :CFG7 add a 3K ohm pull-down to GND --- From Intel Suggestion 08-07-08 01.Page 01-54 : Net Name has #,[x] and space , then change net name definition --- From Layout Suggestion 02.Page 42 : R656,R657,R658 change to connect High side Gate ----- From Power Suggestion 03.Page 04 : Added test point symbol in net TP_SKTOCC# 04.Page 08 : Added test point symbol in U11 pin AT35,AT1,B1,A35 05.Page 08 : Added test point symbol in all TP_.* net 06.Page 14 : (R52/54/55/56) & (R57/58/59/60) combine use RN(0402) 07.Page 15 : eSATA signal (sata3) should be swap with SATA4 signal (RAID Mode issue) 08.Page 15 : Added test point symbol in net TP_SATA_* , TP_HDA_DOCK_RST#, U3A pin A34,F34 09.Page 15 : U4,R85,C118,LED1 should be no_stuff by default 10.Page 34 : U22 pin 55,56 added Series resistor (33 ohm) 11.Page 37 : EC37 change C16 22uF/6.3V 0805 and C372 change 22uF/6.3V 0805 12.Page 37 : C349,C350,C351,C352 can be change use one 270uF/16V solid Cap (OS-CON) 13.Page 50 : The port 80 connector can be remove to Page36 14.Page 50 : The VGA Connector ESD protect(Vport) can be change to use ESD-IP4220(D0G-0422003-P03) 15.Page 5,17,31,32 : C47,C276,C277,C278,C279,C172,C295,C296 From 4.7uF/6.3V(0805) change to 0603 pkg (C11-4757013-M09) 16.Page 5,13,14 : C46,C56,C58,C60,C77,C79,C81 From 2.2uF(0805) change to use 0603 pkg(C11-2257013-W08) 08-13-08 01.Page 18 : Add R55,R332 on net name : DPD_HPD and DPC_HPD ---- From Intel checklist 02.Page 20 : R156 From 10K ohm Change 1K ohm ---- From RED FORT Suggestion 03.Page 16 :Net name - CLK_MINICARD1_OE_L and CLK_MINICARD2_OE_L connect 10Kohm to +V3.3S---- From Check list Suggestion 03.Page 16 :Net name - CLK_MINICARD1_OE_L and CLK_MINICARD2_OE_L connect 10Kohm to +V3.3S---- From Check list Suggestion	08-15-08 01.Page 27 : Change EC30,EC34 package - D type 02.Page 27 : Change EC32,EC33,EC38,EC39,EC31,EC5,EC4,EC47 package - D type 03.Page 31 : Change EC51,EC52,EC53 package - D type , , 47uF/16V 08-18-08 Page28: remove JUSB3 & JUSB4 connector (to save more space for PCB) Page52: added R87,R93,R94,R334 * modify all 100uF CAP. Library Page31: Remove JHDA1 (to save more space for PCB) 08-19-08 01.Page 49,50 : DVI connector Change VGA connector ---- From Intel Suggestion 02.Page 04 : Stuff R10 ---- From Intel Check list 03.Page 15 : Remove R82,R83 ---- From Intel Check list 04.Page 15 : Add R82 33 ohm on SPI_MISO ---- From Intel Check list 05.Page 33 : R296,R302 From 1K ohm Change 3.3K ohm ---- From Intel Check list 06.Page 20 : Add R83 10K ohm pull-up +3.3S , and no stuff R173 ---- From Intel Check list 07.Page 20 : MiniPCIE1 and MiniPCIE2 wake up on LAN control by GPIO1 and GPIO7 , , Change GPIO8 and GPIO15 08.Page 42 : 100 ohm +1k pull-up to VCCSENSE and VSSSENSE ?? -- Intersil reference design for NB solution pull-up 10 ohm on VCCSENSE and pull-down 10 ohm on VSSSENSE ----- From Intersil Suggestion 08-20-08 01.Page 40 : U29 Pin 13 net name from DDR_DRVH Chabge DDR_DRVH1 02.Page 40 : U29 Pin 12 net name from DDR_LL Chabge DDR_LL1 03.Page 40 : U29 Pin 9 net name from DDR_DRVL Chabge DDR_DRL1 04.Page 37 : EC37 From DIP change to SMD 08-21-08 01.Page 04 : Add serial resistor on net name - BCLK_ITP and BCLK_ITP_L ---- From EMI Suggestion 02.Page 16 : Add serial resistor on net name - CLK_DP_P and CLK_DP_P_L ---- From EMI Suggestion 03.Page 16 : Add serial resistor on net name - CLK_MCH_PEG and CLK_MCH_PEG_L ---- From EMI Suggestion 04.Page 16 : Add serial resistor on net name - CLK_PEGA_P and CLK_PEGA_N ---- From EMI Suggestion 05.Page 16 : Add serial resistor on net name - CLK_PCIE_LAN and CLK_PCIE_LAN_L ---- From EMI Suggestion 06.Page 16 : Add serial resistor on net name - CLK_PCIE_MINICARD1 and CLK_PCIE_MINICARD1_L ---- From EMI Suggestion 07.Page 16 : Add serial resistor on net name - CLK_PCIE_MINICARD2 and CLK_PCIE_MINICARD2_L ---- From EMI Suggestion 08.Page 19 : Add Cap.(No Stuff) to GND on net name - CLK_PCI_SIO ---- From EMI Suggestion 09.Page 19 : Add Cap.(No Stuff) to GND on net name - CLK_PCI_FB ---- From EMI Suggestion 10.Page 19 : Add Cap.(No Stuff) to GND on net name - CLK_PCIF_PORT80 ---- From EMI Suggestion 11.Page 16 : Add Cap.(No Stuff) to GND on net name - CLK_BUF_REF14 ---- From EMI Suggestion 12.Page 16 : Add Cap.(No Stuff) to GND on net name - CLK_PCI_FB ---- From EMI Suggestion 13.Page 36 : Add Cap.(No Stuff) to GND on net name - CLK_PCI_SIO ---- From EMI Suggestion 14.Page 15 : Add Cap.(No Stuff) to GND on net name - SPI_CLK ---- From EMI Suggestion 08-22-08 01.Page 34 : Net Name - CLK_BUF_DOT96_P and CLK_BUF_DOT96_N From U22 Pin 24 ,25 Change to U22 Pin17,18 ---- From Intel Suggestion 02.Page 32 : Add a serial resistor on Net name - LAN_XTAL2 connect to U17 Pin 10 ---- From Intel Suggestion 03.Page 30 : SATA1 Change name - SATA0 ---- From RAID tool Requirement 04.Page 30 : SATA2 Change name - SATA1 ---- From RAID tool Requirement 05.Page 30 : SATA3 Change name - SATA2 ---- From RAID tool Requirement 08-25-08 01.Page 32 : Stuff R265 , and Add R575 no stuff resistor ---- From Intel Suggestion 08-26-08 01.Page 39 : Revise Power Solution for Energy Star ---- From Power Suggestion 02.Page 45 : Revise +V12A to +V12S ---- From Power Suggestion																																							
C																																									
B																																									
A																																									
	5	4	3	2	1																																				
				<table><tr><td colspan="3">EMERALD BAY</td><td colspan="3">Intel Confidential</td></tr><tr><td colspan="6">Title</td></tr><tr><td colspan="6">REVISION HISTORY</td></tr><tr><td>Size</td><td colspan="4">Document Number</td><td>Rev</td></tr><tr><td>A</td><td colspan="4"></td><td>B</td></tr><tr><td>Date:</td><td colspan="4">Tuesday, November 18, 2008</td><td>Sheet 51 of 52</td></tr></table>		EMERALD BAY			Intel Confidential			Title						REVISION HISTORY						Size	Document Number				Rev	A					B	Date:	Tuesday, November 18, 2008				Sheet 51 of 52
EMERALD BAY			Intel Confidential																																						
Title																																									
REVISION HISTORY																																									
Size	Document Number				Rev																																				
A					B																																				
Date:	Tuesday, November 18, 2008				Sheet 51 of 52																																				
	5	4	3	2	1																																				

5	4	3	2	1
08-27-08		09-19-08		
01.Page 26 : Revise CN2 footprint for 1.8V ONFI		01.Page 48 : Change PCB color ,, From Coffee color change Blue color , change material number		
02.Page 13,14 : C72,C73,C74,C75,C93 From 0.1uF change to 1uF ---- From Design guide Suggestion				
03.Page 50 : Stuff Page 50 PCIE to SATA on ES1 chip		10-23-08		
04.Page 01 : Revise BLock Diagram		REV:A --> REV:B		
08-28-08		01.Page 01 : Revise Title Block informations		
01.Page 38 : Revise R665 From 120K ohm 1% change to 10K ohm 1% ---- From Power Suggestion		02.Page 03-09 : Update U1 Symbol from Intel Update data		
02.Page 40 : Revise R383 From 16.9K ohm 1% change to 9.1K ohm 1% ---- From Power Suggestion		03.Page 10 : Remove FAN2		
03.Page 40 : Revise R392 From 16.9K ohm 1% change to 5.1K ohm 1% ---- From Power Suggestion		04.Page 15-23 : Update U3 Symbol from Intel Update data		
04.Page 40 : Revise R393 From 10K ohm 1% change to 8.2K ohm 1% ---- From Power Suggestion		05.Page 15 : Remove Net Name -SATA_RXN4_C,SATA_RXP4_C,SATA_TXN4_C,SATA_TXP4_C,SATA_RXN4,SATA_RXP4,SATA_TXP4,SATA_TXN4,		
05.Page 40 : Revise R395 From 5.49K ohm 1% change to 20.5K ohm 1% ---- From Power Suggestion		06 Page 15 : Remove Net Name - TP_SATA_RXN5,TP_SATA_RXP5,TP_SATA_TXN5,TP_SATA_TXP5 and TP234,TP235,TP236.TP237		
06.Page 39 : Add U45 regulator ---- From Intel DOC 400755 Suggestion		07 Page 16 : Increase R590 between net name -XTAL25_IN and XTAL25_OUT		
07.Page 7 : Add U1 Pin J17 connect M_VREF_DQ_DIMM0 and U1 Pin H17 connect M_VREF_DQ_DIMM1 ---- From Intel DOC 400755 Suggestion		08 Page 16 : Remove TP220,TP221,TP218,TP219,TP224,TP225,TP222,TP223,TP228,TP229,TP226,TP227,TP232,TP233,TP230,TP231		
09-01-08		09 Page 17 : U3 Pin C16 Change net name : PM_RSMRST_PCHL		
01.Page 03-09 : Update U1 Symbol ---- From Intel Suggestion		10 Page 18 : Net name - DPC_HPD increase Hot Plug circuit		
02.Page 15-23 : Update U3 Symbol ---- From Intel Suggestion		11 Page 27 : Net name - +V5A_USBPWR_PN0 short +V5A_L_USBPWR_PN0		
03.Page 26 : Update CN2 footprint		12 Page 27 : Net name - +V5A_USBPWR_PN2 short +V5A_L_USBPWR_PN2		
04.Page 41 : U31 Pin 29 Change connect Digital GND ---- From Power Suggestion		13 Page 28 : Net name - +V5A_USBPWR_PN4_PN5 short +V5A_L_USBPWR_PN4_PN5		
05.Page 39 : U25 Pin 33 Change connect Digital GND ---- From Power Suggestion		14 Page 28 : Net name - +V5A_USBPWR_PN6_PN7 short +V5A_L_USBPWR_PN6_PN7		
06.Page 46 : Update U40,U42 footprint		15 Page 29 : MINIPCI1 Pin 2,41,43,52 From +V3.3A change to +V3.3S		
09-03-08		16 Page 29 : MINIPCI2 Pin 2,41,43,52 From +V3.3A change to +V3.3S		
01.Page 48 : Add Heatsink HK1 for U3		17 Page 30 : Remove SATA4 , the SATA4 signal trace change to CN4B connected SATA4 signal trace		
02.Page 46 : Update U34 Layout Footprint		18 Page 31 : U16 Pin 9 From +V1.5S change to +V3.3S --- From Realtek Suggestion		
03.Page 39 : Update U25 Layout Footprint		19 Page 31 : U16 Pin 4 add R265 no stuff ---- From Realtek Suggestion		
04.Page 34 : Update U22 Material data				
09-04-08		10-27-08		
01.Page 24 : Swap trace on Pin of L13 , L17 ---- From Layout Suggestion		01.Page 39 : Add EC54 DIP need to move near CHOK2		
02.Page 11 : Swap trace on Pin of RN9 ---- From Layout Suggestion		10-28-08		
03.Page 36 : Swap trace on Pin of RN6 ---- From Layout Suggestion		01.Page 25 : JLVDS1 Pin 1~ 6 From +V12S Change to LCD_VDD		
09-08-08		02.Page 25 : JLVDS1 Pin 7 From +V3.3S Change to GND		
01.Page 42 : Remove R642 ,R623 ; Then Net Name : ISL_PW3 directly connect PWM3 ---- From Power Suggestion		03.Page 25 : JLVDS1 Pin 9 From LCD_VDD Change to GND		
02.Page 11 : Change RN8 , RN9 Net connect for layout ---- From Layout Suggestion		10-29-08		
03.Page 19 : Change RN2 Net connect for layout ---- From Layout Suggestion		01.Page 40 :Net name : +V1.1S_VTT add EC9 , EC10 ----- Power team Suggestion		
04.Page 35 : Change RN14 Net connect for layout ---- From Layout Suggestion		10-31-08		
05.Page 35 : Change RN13 Net connect for layout ---- From Layout Suggestion		01.Page 42 : Modify current sensor		
06.Page 48 : Add HK2(CPU Bottom) on U1		11-07-08		
09-09-08		01.Page 49 : Add U47,U52 in Hsync and Vsync		
01.Page 49 : VGA1 from N51-15F0391-K06 change to N51-15F0391-A10 ---- From Purchaser Suggestion				
09-10-08				
01.Page 31 : CON8 Pin 4 from MIC_IN_R change MIC_IN_L ; Pin 1 from MIC_IN_L change MIC_IN_R				
02.Page 31 : CON7 Pin 4 from LINE_OUT_R change LINE_OUT_L ; Pin 1 from LINE_OUT_L change LINE_OUT_R				
03.Page 44 : Net Name : PM_PWRBTN_L add a 10K ohm pull-high to +V3.3A				
04.Page 42 : Remove C493 and net name : COMP ---- From Power Suggestion				
09-11-08				
01.Page 30 : CN4 Pin S5 , S6 is NPTH via hole , not connect				
02.Page 48 : MH3 from connect net : GND Change to connect GNDF ---- From Layout Suggestion				
09-12-08				
01.Page 25 : Add J19 for LVDS Panel light control				
02.Page 33 : Revise R294 connect SPI_WP_L				
03.Page 48 : Revise MH3 net change to No connect				
04.Page 16, 32 : X2 , X3 From D04-1001100-E24 Change to D04-1001100-F07(AVL:D04-1001100-T16,D04-1001100-T02) ---- From Puschaser Suggestion				
05.Page 48 : Del SIP3 , SIP4 , SIP6				
06.Page 44 : JFP1 Change package Pitch 2.0mm				
07.Page 36 : J16 Change package Pitch 2.0mm				
09-13-08				
01.Page 24 : C194 pin 1 and 2 connect together , Change net name				
02.Page 24 : C195 pin 1 and 2 connect together , Change net name				
09-14-08				
01.Page 48 : Add Optical point FM5 and FM6 ---- From Factory Suggestion				
01.Page 32 : R283 change net - +LAN_VCT ---- From Intel Suggestion				
09-18-08				
01.Page 48 : Add PCB Material number				
5	4	3	2	1

EMERALD BAY				Intel Confidential	
Title					
REVISION HISTORY					
Size		Document Number			Rev
Custom					B
Date:		Tuesday, November 18, 2008		Sheet	52 of 52